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User's Guide

Publication number E3472-97001
Second edition, March 1997

For Safety information, Warranties, and Regulatory information, see the pages preceding the table of contents.

HP E3472A/73A Emulator
for SH7040/50

Notice

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Printing History

New editions are complete revisions of the manual. The date on the title page changes only when a new edition is published.

A software code may be printed before the date; this indicates the version level of the software product at the time the manual was issued. Many product updates and fixes do not require manual changes, and manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual revisions.

Edition 1

E3472-97000, Oct. 1996

Edition 2

E3472-97001, Mar. 1997

Certification

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Institute of Standards and Technology, to the extent allowed by the Institution's calibration facility, or to the calibration facilities of other International Standards Organization members.

Warranty

This Hewlett-Packard instrument product is warranted against defects in material and workmanship for a period of one year from the date of shipment, except that in the case of certain components listed in *General Information* of this manual, the warranty shall be for the specified period. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products that prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instruction when property installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

Limitation Of Warranty

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside the environmental specifications for the product, or improper site preparation or maintenance.

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The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract, tort, or any other legal theory.

Assistance

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

Safety Summary

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific WARNINGS elsewhere in this manual may impair the protection provided by the equipment. In addition it violates safety standards of design, manufacture, and intended use of the instrument. *The Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.*

Note The HP E3472A/73A complies with INSTALLATION CATEGORY I and POLLUTION DEGREE 2 in IEC1010-1. The HP E3472A/73A is INDOOR USE product.

Note LEDs in this product are Class 1 in accordance with IEC825-1.

CLASS 1 LED PRODUCT

Ground The Instrument

To avoid electric shock hazard, the AC/DC adapter must be connected to a safety earth ground by the supplied power cable with earth blade.

DO NOT Operate in an Explosive Atmosphere

Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a safety hazard.

Keep Away From Live Circuits

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with the power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT Substitute Parts or Modify Instrument

Because of the danger of introducing additional hazards, do not install substitute parts or perform unauthorized modifications to the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

Dangerous Procedure Warnings

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

Warning Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting this instrument.

Power Requirements

The HP E3472A/73A requires the following power source:

Voltage : 90 to 132 Vac, 198 to 264 Vac

Frequency : 47 to 63 Hz

Power : 300 VA maximum

Power Cable

In accordance with international safety standards, this instrument is equipped with a three-wire power cable. When connected to an appropriate ac power outlet, this cable grounds the instrument frame.

The type of power cable shipped with each instrument depends on the country of destination. Refer to Figure 1 for the part numbers of the power cables available.

Warning

For protection from electrical shock, the power cable ground must no be defeated.

The power plug must be plugged into an outlet that provides a protective earth ground connection.

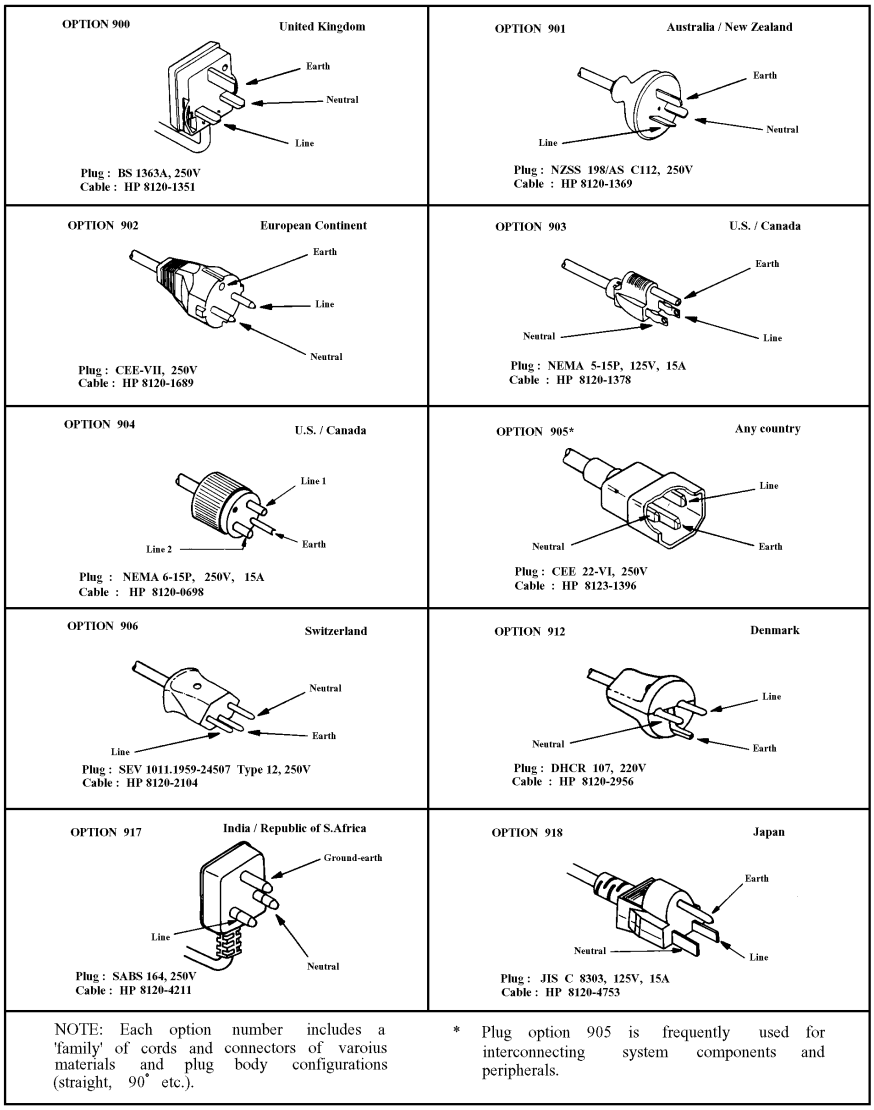


Figure 1. Power Cords Available for Each Destination

Safety Symbols

General definitions of safety symbols used on equipment or in manuals are listed below.

Instruction manual symbol: the product is marked with this symbol when it is necessary for the user to refer to the instruction manual.

Alternating current.

Direct current.

On(Supply).

Off(Supply).

Warning This warning sign denotes a hazard. If calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in injury or death to personnel.

Caution This caution sign denotes a hazard. If calls attention to a procedure, practice, condition or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product.

Note This note sign denotes important information. If calls attention to a procedure, practice, condition or the like, which is essential to highlight.

Outline of this manual

Chapter 1 describes the product overview and its outer features.

Chapter 2 lists the contents of the product.

Chapter 3 shows you how to assemble the Emulator and install memory modules.

Chapter 4 shows you how to configure LAN parameters to connect the Emulator to the host computer.

Chapter 5 shows you how to connect the Emulator to your target system.

Chapter 6 describes instructions in designing target system.

Chapter 7 shows you how to use the Emulator with a logic analyzer connected.

Chapter 8 describes the specifications and characteristics of the product.

Chapter 9 shows you how to update the firmware of the Emulator.

Chapter 10 shows you, if a problem occurs when working with the Emulator, how to isolate its causes.

Appendix A lists the register classes available with the Emulator.

Contents

1

Product Overview

Product Overview

The HP E3472A/73A Emulator provides distributed emulation environment for the Hitachi SH7040/50 Series processors. Depending on size and requirements of your development, you can use it either as a simple emulator working standalone, or as a powerful debugging environment by connecting it to a logic analyzer.

Hooking up the HP E3472A/73A Emulator to an HP's logic analyzer enables high-speed real-time tracing. You can control the emulator and logic analyzer through the HP E3755A/56A Debug User Interface, allowing you to operate the emulation environment with a feel similar to conventional debuggers.

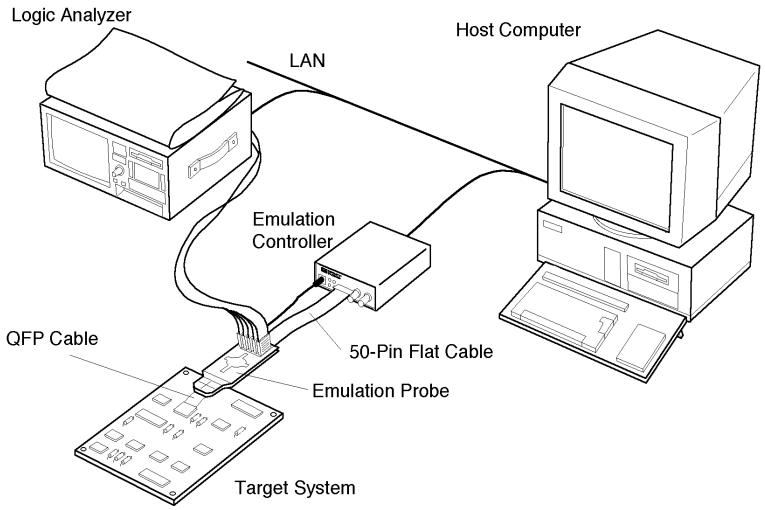
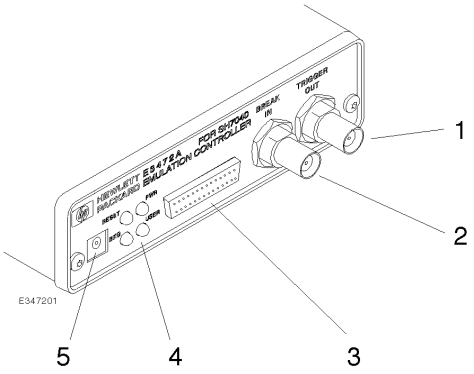


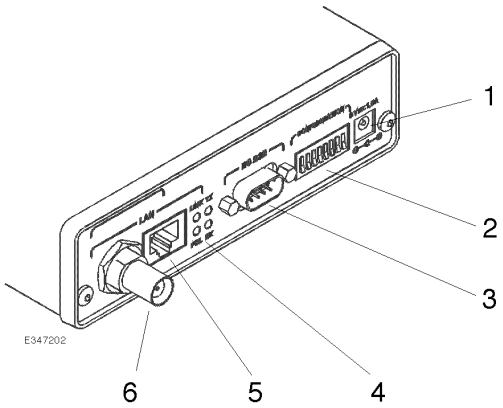
Figure 1-1. Distributed Emulation Environment with HP E3472A/73A

Emulator Components

Emulation controller

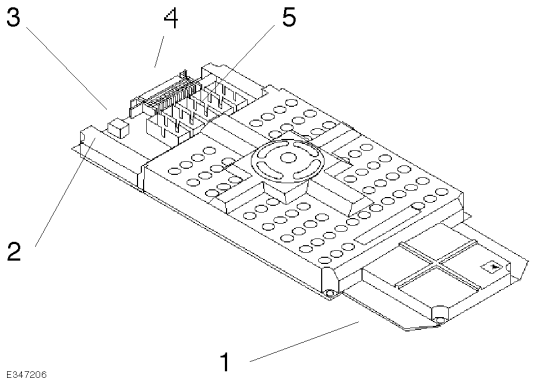


1. TRIGGER OUT connector	Sends out the trigger signal.
2. BREAK IN connector	Receives the trigger signal from the logic analyzer.
3. 50-pin connector	Connected to the emulation probe through the 50-pin flat cable.
4. Status LEDs	Indicate the operating status of the emulation controller.
5. Auxiliary power connector	Supplies power to the emulation probe.



1. Power connector	Connects the power cable. Connecting/disconnecting the power cable will switch ON/OFF the emulator.
2. DIP switches	Configure the settings of the Emulator. Instructions are printed on the bottom of the emulation controller.
3. RS-232 connector	Connects the RS-232 cable to communicate with the host computer via the serial connection.
4. LAN status LEDs	Indicate the communication status of the Emulator working on the LAN.
5. LAN connector (10BASE-T)	Connects the LAN cable when the Emulator communicates with the host computer via 10BASE-T LAN.
6. LAN connector (10BASE2)	Connects the LAN cable when the Emulator communicates with the host computer via 10BASE2 LAN.

Emulation probe



1. PGA connector	Connects to the QFP socket/adapter seated on the target system.
2. Power LED	Indicates that power is supplied to the emulation probe.
3. Power connector	Connects the auxiliary power cable from the emulation controller.
4. 50-pin connector	Connected to the emulation controller through the 50-pin flat cable.
5. Pod connector	Connects the pods of the logic analyzer.

Usage - Quick Guide

The target connection

The HP E3472A/73A Emulator connects to your target system via a flexible cable. The cable plugs into a QFP socket/adapter on the target system.

The host computer connection

The HP E3472A/73A Emulator can communicate with a host computer via a LAN connection (10 BASE-T or 10 BASE2).

The configuration switches

Use the DIP switches on the emulation controller to configure communication to the host computer. There is a guide to these switches on the bottom of the emulation controller.

The status LEDs

LEDs show the status of the power supply, the target system, and the connection to the host computer.

2

Contents of HP E3472A/73A

Contents of HP E3472A/73A

This chapter provides you the information necessary for the followings.

- Incoming Inspection
- Instruction for Cleaning

Incoming Inspection

WARNING

To avoid hazardous electrical shock, do not turn on the HP E3472A/73A when there are signs of shipping damage to any portion of the outer enclosure (for example, covers, or panel).

Inspect the shipping container for damage. If the shipping container of cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the HP E3472A/73A Processor Probe has been checked mechanically and electrically. The contents of the shipment should be as listed in next page. If the contents are incomplete, if there is mechanical damage or defect, or if the HP E3472A/73A does not pass the performance verification test, notify the nearest Hewlett-Packard office. If the shipping container is damaged, or the cushioning materials shows signs of unusual stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for the carrier's inspection.

Contents (HP E3472A)

Description	Qty.	HP Part Number
SH7040 emulation probe board	1	E3472-66501
Emulation probe top cover	1	E3472-04101
Emulation probe bottom cover	1	64783-04102
SH7040 demo board	1	E3472-66502
Emulation controller	1	E3472-65001
50-pin flat cable	1	E3496-61601
AUX power cable	1	E3496-61602
AC/DC adapter	1	0950-3043
Power cable	1	8120-4753
3-wire to 2-wire adapter	1	5080-3149
Loop-back board	1	E3496-66502
Coaxial cable (120 cm)	1	8120-1840 [1]
Thin LAN T-connector	1	92227N
Thin LAN 50 ohm terminator (2 pcs)	1	92227P
Plastic rivet kit	1	64748-68700
Others (including manuals)		

1 This cable is not suitable for LAN but for trigger input to the Emulator or performance verification test. Do not use this as a LAN cable.

Contents (HP E3473A)

Description	Qty.	HP Part Number
SH7050 emulation probe board	1	E3473-66501
Emulation probe top cover	1	E3472-04101
Emulation probe bottom cover	1	64783-04102
SH7050 demo board	1	E3473-66502
Emulation controller	1	E3473-65001
50-pin flat cable	1	E3496-61601
AUX power cord	1	E3496-61602
AC/DC adapter	1	0950-3043
Power cord	1	8120-4753
3-wire to 2-wire adapter	1	5080-3149
Loop-back board	1	E3496-66502
Coaxial cable (120 cm)	1	8120-1840 [1]
Thin LAN T-connector	1	92227N
Thin LAN 50 ohm terminator (2 pcs)	1	92227P
Plastic rivet kit	1	64748-68700
Others (including manuals)	1	

1 This cable is not suitable for LAN but for trigger input to the Emulator or performance verification test. Do not use this as a LAN cable.

Instruction for Cleaning

For cleaning the case and operation panel of the Emulation Controller, wipe with soft cloth that is soaked with water and wrung tightly, without undue pressure.

Ventilation Requirements

To ensure adequate ventilation, make sure that there is adequate clearance around the emulation controller, the emulation probe, and the AC/DC adapter.

3

Setting up the Emulator

Setting up the Emulator

Caution

To prevent the emulator and the target system from being damaged, be sure to follow the cautions below when handling them.

- When connecting/disconnecting the emulation controller and emulation probe, first disconnect the power cable from the emulation controller to stop supplying power and then the emulation probe from the target system.
- To prevent the emulator from being damaged by static electricity, store and use the emulator in a place resistant to static electricity.
- When supplying power to the emulator, check that the emulation probe is plugged into the target system or demo board.

Before connecting the Emulator to the power supply, be sure to follow the instructions below regarding the power cable.

The HP E3472A/73A Emulator is shipped from the factory with a power supply and cord appropriate for your country. Use only the supplied HP power supply and cord. Failure to use the proper power cable could result in electric shock.

WARNING

For protection from electrical shock, the power cable ground must not be defeated.

The power plug must be plugged into an outlet that provides a protective earth ground connection.

Procedure

1. Connect the power supply cord between the emulation probe and emulation controller.
2. Connect the 50-pin ribbon cable between the emulation probe and the emulation controller.
3. Plug the emulation probe into the target system

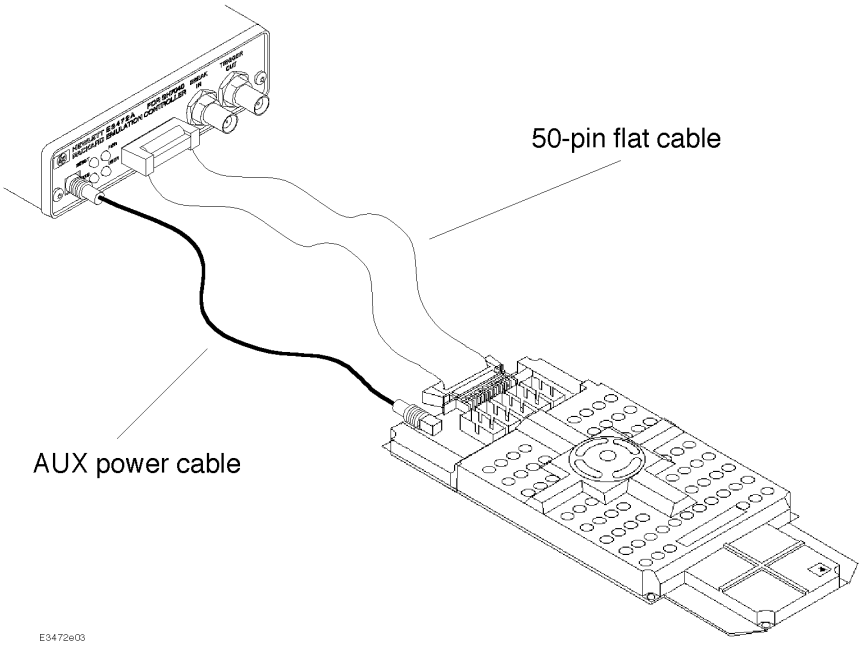
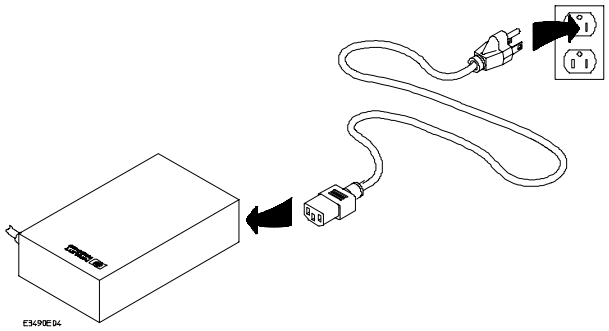


Figure 3-1. Connecting the Emulation Controller and the Emulation Probe

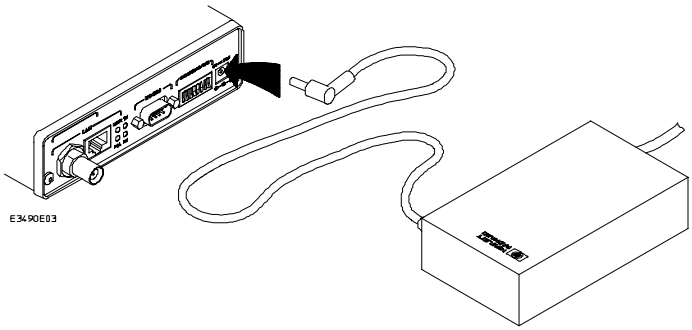
To connect the power cord and turn on the HP E3472A/73A Emulator

The HP E3472A/73A Emulator does not have an On/Off switch. To turn the HP E3472A/73A Emulator on or off, plug or unplug it from the power supply.

1 Plug the power cable into the adapter and outlet.



2 Connect the 5-V power cable to the receptacle in the rear panel of the HP E3472A/73A Emulator.



Note The power lights on the emulation controller and the emulation probe are lit, indicating the HP E3472A/73A Emulator is powered on. Note that the Emulator does not have power switch.

To test the HP E3472A/73A Emulator

If this is the first time you have used the HP E3472A/73A Emulator, you should run the built-in performance verification test before you connect to a target system.

For details on the procedure of the performance verification test, see page 108.

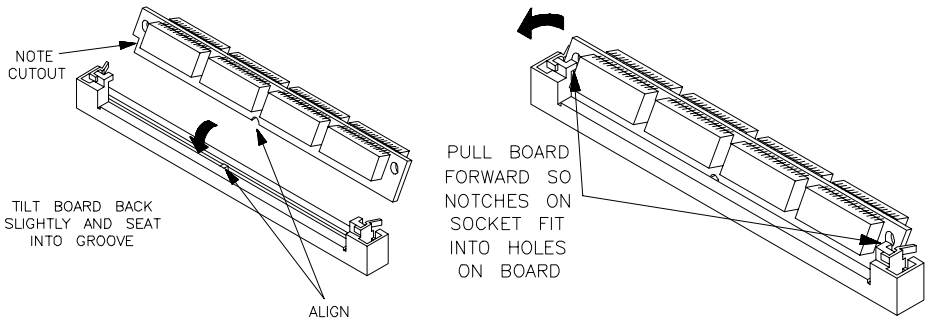
Installing the Emulation Memory Module

There are three types of emulation memory modules that can be inserted into sockets on the probe.

Note Installing the emulation memory requires the plastic rivet kit (HP Parts No. 64748-68700).

1. Remove plastic rivets that secure the plastic cover on the top of the emulator probe, and remove the cover. The bottom cover is only removed when you need to replace a defective active probe on the exchange program.
2. Insert emulation memory module on the emulation probe. There is a cutout on one side of the memory modules so that they can only be installed one way.

   To install memory modules, place the memory module into the socket groove at an angle. Firmly press the memory module into the socket to make sure it is completely seated. Once the memory module is seated in the connector groove, pull the memory module forward so that the notches on the socket fit



into the holes on the memory module. There are two latches on the sides of the socket that hold the memory module in place.

3 Replace the plastic cover, and insert new plastic rivets to secure the cover.

4

Connecting to the Host Computer

Connecting to the Host Computer

To use the HP E3472A/73A Emulator you need to:

- Connect the HP E3472A/73A Emulator to the target system (described in the next chapter)
- Connect the HP E3472A/73A Emulator to a power source. See "Assembling the Emulator" for the connection procedure.
- Power on the target system
- Connect the HP E3472A/73A Emulator to the host computer via a LAN
- Set up the host software

If you plan to use the HP E3472A/73A on a PC, you will need to set up a serial connection to set the IP address for LAN.

As a debugger controlling the Emulator, you can use the HP E3755A/56A Debug User Interface on a UNIX workstation or a PC.

Note When supplying power to the emulator, check that the emulation probe is plugged into the target system or demo board.

Setting Up a LAN Connection

The HP E3472A/73A Emulator has two LAN connectors:

- A BNC connector that can be directly connected to a IEEE 802.3 Type 10BASE2 cable (ThinLAN). When using this connector, the HP E3472A/73A Emulator provides the functional equivalent of a Medium Attachment Unit (MAU) for ThinLAN.
- An IEEE 802.3 Type 10BASE-T connector.

Use either the 10BASE2 or the 10BASE-T connector. Do *not* use both. The HP E3472A/73A Emulator will not work with both connected at the same time.

You must assign an IP address (Internet address) to the HP E3472A/73A Emulator before it can operate on the LAN. You can also set other network parameters such as a gateway address. The IP address and other network parameters are stored in nonvolatile memory within the HP E3472A/73A Emulator.

The HP E3472A/73A Emulator automatically sets a subnet mask based on the subnet mask used by other devices on the network.

You can configure LAN parameters in any of the following ways:

- Using the built-in terminal interface. This is the most reliable method.
- Using ipconfig700. The ipconfig700 program is supplied with the HP E3755A/56A Debug User Interface on HP and Sun workstations.
- Using BOOTP. BOOTP is part of the HP-UX operating systems.

To obtain an IP address

1 Obtain the following information from your local network administrator or system administrator:

- An IP address for the HP E3472A/73A Emulator.
- The gateway address.

The gateway address is an IP address and is entered in integer dot notation. The default gateway address is 0.0.0.0, which allows all connections on the local network or subnet. If connections are to be made to workstations on other networks or subnets, this address must be set to the address of the gateway machine.

2 Find out whether port numbers 6470 and 6471 are already in use on your network.

The host computer interfaces communicate with the HP E3472A/73A Emulator through two TCP service ports. The default base port number is 6470. The second port has the next higher number (default 6471).

The default numbers (6470, 6471) can be changed if they conflict with some other products on your network. TCP service port numbers must be greater than 1024. If you change the base port, the new value must also be entered in the /etc/services file on the host computer. For example, you could modify the line:

hp64700 6470/tcp

To change the port numbers, see page 23. If you have already set the IP address, you can use a telnet connection instead of a serial connection to connect to the HP E3472A/73A Emulator.

Also you have to be sure that the port number you use does not conflict with the one for the logic analyzer.

3 Write down the link-level address of the HP E3472A/73A Emulator.

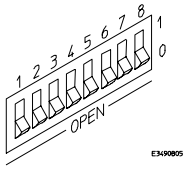
You will need this address if you use BOOTP or ipconfig700 to set the IP address.

The link-level address (LLA) is printed on a label above the LAN connectors on the HP E3472A/73A Emulator. This address is configured in each HP E3472A/73A Emulator shipped from the factory and cannot be changed.

To configure LAN parameters using the built-in terminal interface

1. **Set configuration switches S1 through S4 to CLOSED, and set the other switches as appropriate for your serial interface.**

   Switch settings are printed on the bottom of the HP E3472A/73A Emulator. If you will use a baud rate of 9600 baud, set the switches like this:



2. **Connect an ASCII terminal (or terminal emulator) to the HP E3472A/73A Emulator's RS-232 port with a 9-pin RS-232 cable.**

   Complete instructions for setting up a serial connection are described at "Setting Up a Serial Connection" in this chapter.

3. **Plug in the HP E3472A/73A Emulator's power cord. Press the terminal's <RETURN> key a couple times. You should see a "R>", "p>" or "c>" prompt.**

   At this point, you are communicating with the HP E3472A/73A Emulator's built-in terminal interface.

4. **Display the current LAN configuration values by entering the lan command:**

```
R>lan
lan is disabled
lan -i 0.0.0.0
lan -g 0.0.0.0
lan -p 6470
Ethernet Address : 08000903212f
```

   The "lan -i" line shows the current IP address (IP address) of the HP E3472A/73A Emulator.

   The "Ethernet Address", also known as the link-level address, is preassigned at the factory, and is printed on a label above the LAN connectors.

5. **Enter the following command:**

```
lan -i <internet> [-g <gateway>] [-p <port>]
```

   The lan command parameters are:

`-i <internet>` The IP address which you obtained from your network administrator.

`-g <gateway>` The gateway address. Setting the gateway address allows access outside your local network or subnet.

`-p <port>` This changes the base TCP service port number.

The default numbers (6470, 6471) can be changed if they conflict with some other products on your network. TCP service port numbers must be greater than 1024. If you change the base port, the new value must also be entered in the /etc/services file on the host computer. For example, you could modify the line:

hp64700 6470/tcp

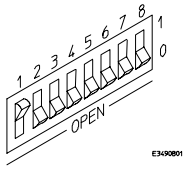
6 Disconnect the power cord from the HP E3472A/73A Emulator, and connect the the HP E3472A/73A Emulator to your network.

This connection can be made by using either the 10BASE-T connector or the 10BASE2 (BNC) connector on the HP E3472A/73A Emulator. Do not use both connectors at the same time.

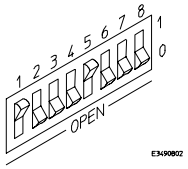
7 Set the configuration switches to indicate the type of connection that is to be made.

Switch S1 must be set to OPEN, indicating that a LAN connection is being made.

Switch S5 should be 1 if you are connecting to the BNC connector:



Switch S5 should be 0 if you are connecting to the 10BASE-T connector:



Set all other switches to CLOSED.

8 Connect the power cord to the HP E3472A/73A Emulator.

9 Verify your HP E3472A/73A Emulator is now active and on the network. See "To verify LAN communications" in this chapter.

Once you have set a valid IP address, you can use the telnet utility to connect to the HP E3472A/73A Emulator, and use the lan command to change LAN parameters.

Example

For example, to assign an IP address of 192.6.94.2 to the HP E3472A/73A Emulator, enter the following command:

```
R>lan -i 192.6.94.2
```

The IP address and any other LAN parameters you change are stored in nonvolatile memory and will take effect the next time the HP E3472A/73A Emulator is powered off and back on again.

See Also

"Solving Problems," page 103, if you have problems verifying LAN communication.

To configure LAN parameters using "ipconfig700"

When you are using HP 9000/700 computer or Sun SPAPCsystem with HP B3755A/56A installed in it, you can use ipconfig700 command to configure LAN parameters.

The ipconfig700 command sets the IP address and gateway address for the HP E3472A/73A Emulator. An IP address must be configured before a network interface connection can be made.

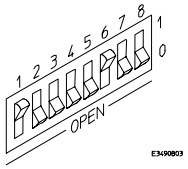
The ipconfig700 command cannot be used if your workstation is running a bootp daemon. If this is the case, use BOOTP to configure LAN parameters. To determine if BOOTP is enabled on your computer, see "To configure LAN parameters using BOOTP" in this chapter.

The following steps need to be taken when configuring the network parameters with ipconfig700.

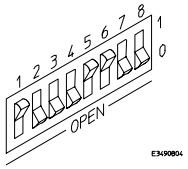
1. **Connect the HP E3472A/73A Emulator to your network. This connection can be made by using either the 10BASE-T connector or the 10BASE2 BNC connector on the HP E3472A/73A Emulator.**
2. **Set the configuration switches to indicate the type of connection that is to be made.**

   Switch S1 must be set to OPEN, indicating that a LAN connection is being made. Switch S6 must bet set to OPEN, to allow programming of the LAN parameters.

Switch S5 should be 1 if you are connecting to the BNC connector:



Switch S5 should be 0 if you are connecting to the 10BASE-T connector:



Set all other switches to CLOSED.

3. Turn ON power to the HP E3472A/73A Emulator.
4. Wait at least 20 seconds for the HP E3472A/73A Emulator to connect to the LAN.
5. Become the root user on the system from which you wish to configure the HP E3472A/73A Emulator.
6. Enter the following command:

   ipconfig700 -l <link> **-i** <internet> [**-g** <gateway>]

   The ipconfig700 parameters are:

   `-l <link>` The link-level address. Enter any letters in the address in upper case.

   `-i <internet>` The IP address.

   `-g <gateway>` The gateway address.

   If the ipconfig700 command is entered without any options, the program interactively prompts for the necessary information.

7. Disconnect the power cable from the emulation controller. Set switch S6 back to CLOSED and connect the power cable again.
8. Verify your HP E3472A/73A Emulator is now active and on the network. See "To verify LAN communications" in this chapter.

Example

If the link-level address on your HP E3472A/73A Emulator read 08000F090F30, and your system administrator gave you the IP address 192.35.12.6, you could enter the following command:

```
$ ipconfig700 -l 08000F090B30 -i 192.35.12.6 <RETURN>
```

Because no gateway address was entered, this value would default to 0.0.0.0. When the IP address is successfully programmed, ipconfig700 will display the HP E3472A/73A Emulator version information.

Limitations of ipconfig700

The ipconfig700 command generally will not work if:

- the workstation and the HP E3472A/73A Emulator are on different subnets

OR

- a BOOTP daemon running elsewhere on your network is configured to respond to the link-level address of the HP E3472A/73A Emulator.

To configure LAN parameters using BOOTP

This method is applicable only if your HP-UX workstation is already running bootpd, the BOOTP daemon. The ipconfig700 command does the same thing as BOOTP and is easier to use.

The BOOTP software is shipped with HP-UX version 8.0 or later.

1 Make sure that your host computer supports BOOTP.

If the following commands yield the results shown below, your machine supports the BOOTP protocol.

```
$ grep bootp /etc/services
bootps      67/udp
bootpc      68/udp
$ grep bootp /etc/inetd.conf
bootps  dgram  udp  wait    root  /etc/bootpd   bootpd
```

If the commands did not yield the results shown, you must either add BOOTP support to your workstation or use a different method to configure the HP E3472A/73A Emulator LAN parameters.

2 Add an entry to the host BOOTP database file, /etc/bootptab. For example:

```
# Global template for options common to all HP 64700
emulators.
# Gateway addresses can be specified differently if
# necessary.

hp64700.global:\
        :gw=0.0.0.0:\
        :vm=auto:\
        :hn:\
        :bs=auto:\
        :ht=ether

# Specific emulator entry specifying hardware address
# (link-level address) and ip address.

hpprobe.div.hp.com:\
        :tc=hp64700.global:\
        :ha=080009090B0E:\
        :ip=192.6.29.31
```

In the example above, the "ha=080009090B0E" identifies the link-level address of the HP E3472A/73A Emulator.

The "ip=192.6.29.31" specifies the IP address that is assigned to the HP E3472A/73A Emulator.

The node name is "hpprobe.div.hp.com".

For additional information about using bootpd, refer to the HP-UX man pages.

3 Connect the HP E3472A/73A Emulator to your network.

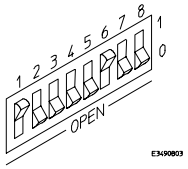
This connection can be made by using either LAN connector on the HP E3472A/73A Emulator.

4 Set the configuration switches to indicate the type of connection that is to be made.

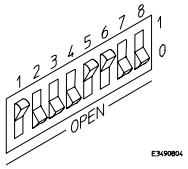
Switch S1 must be set to OPEN, indicating that a LAN connection is being made.

Switch S6 must be set to OPEN to enable BOOTP mode.

Switch S5 should be set to CLOSED if you are connecting to the BNC connector



Switch S5 should be set to OPEN if you are connecting to the 10BASE-T connector.



Set all other switches to CLOSED.

5 Connect the power cord to the HP E3472A/73A Emulator.

Verify that the power light stays on after 10 seconds.

The IP address will be stored in EEPROM.

6 Disconnect the power cable from the emulation controller. Set switch S6 back to CLOSED and connect the power cable again.

Do this so that the HP E3472A/73A Emulator does not request its IP address each time power is cycled. The IP address is stored in EEPROM, so BOOTP does not need to be run again. Leaving this switch on will result in slower performance, increased LAN traffic, and even failure to power up (if the BOOTP server becomes inactive).

7 Verify your HP E3472A/73A Emulator is now active and on the network. See "To verify LAN communications" in this chapter.

To set the 10BASE-T configuration switches

Set switches S7 and S8 to CLOSED unless one of the following conditions is true:

- **If the LAN cable exceeds the standard length, set switch S7 to OPEN.**
  The HP E3472A/73A Emulator has a switch-selectable, twisted-pair receiver threshold. With switch S7 set to OPEN, the twisted-pair receiver threshold is lowered by 4.5 dB. This should allow you to use cable lengths of up to about 200 meters. If you use a long cable, you should consult with your LAN cabling installer to ensure that:
  - The device at the other end of the cable has long cable capability, and
  - The cable is high-grade, low-crosstalk cable with crosstalk attenuation of greater than 27.5 dB.

  When switch S7 is set to CLOSED, the LAN port operates at standard 10BASE-T levels. A maximum of 100 meters of UTP cable can be used.
- **If your network doesn't support LINK BEAT integrity checking or if the HP E3472A/73A Emulator is connected to a non 10BASE-T network set this switch to LINK BEAT OFF (0 or OPEN).**
  In normal mode (switch S8 set to CLOSED), a link integrity pulse is transmitted every 15 milliseconds in the absence of transmitted data. It expects to receive a similar pulse from the remote MAU. This is the standard link integrity test for 10BASE-T networks. If your network doesn't support the LINK BEAT integrity checking or if the Emulator is used on a non 10BASE-T network set this switch to LINK BEAT OFF (OPEN).

Note **Setting switch S8 to OPEN when Link Beat integrity checking is required by your network will cause the remote MAU to disable communications.**

To verify LAN communications

1. Verify your HP E3472A/73A Emulator is now active and on the network by issuing a **telnet** to the IP address.

   This connection will give you access to the HP E3472A/73A Emulator's built-in terminal interface.

2. To view the LAN parameters, enter the **lan** command at the terminal interface prompt.
3. To exit from this telnet session, type <CTRL>D at the prompt.

   The best way to change the HP E3472A/73A Emulator's IP address, once it has already been set, is to telnet to the HP E3472A/73A Emulator and use the terminal interface lan command to make the change. Remember, after making your changes, you must cycle power or enter a terminal interface init -p command before the changes take effect. Doing this will break the connection and end the telnet session.

If You Have Problems

If you encounter problems, refer to the "Solving Problems" chapter (page 99).

Example

```
$ telnet 192.35.12.6
R>lan
lan is enabled using TP
  lan -i 192.35.12.6
  lan -g 0.0.0.0
  lan -p 6470
  Subnet Mask: 255.255.255.0
  Ethernet Address: 08000F090B30
```

Setting Up a Serial Connection

To set up a serial connection, you will need to:

- Set the serial configuration switches
- Connect the HP E3472A/73A Emulator to the RS-232 interface
- Connect a serial cable between the host computer and the HP E3472A/73A Emulator
- Verify communications

Serial connections on a workstation

You should not use a serial connection on a workstation, except to set LAN parameters.

Serial connections on a PC

You should not use a serial connection on a PC, except to set LAN parameters or to update the HP E3472A/73A firmware.

To set the serial configuration switches

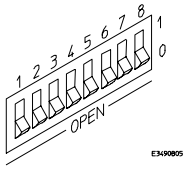
1. Set switch S1 to CLOSED (RS-232).
2. Set switches S2-S4 to CLOSED.
3. Set switch S5 to CLOSED (HW HANDSHAKE ON) if your serial interface uses the DSR:CTS/RTS lines for flow control. Set S5 to OPEN (HW HANDSHAKE OFF) if your serial interface uses software flow control (XON/XOFF).

   If your serial interface supports hardware handshaking, you should use it (set switch S5 to CLOSED). Hardware handshaking will make the serial connection much more reliable.
4. Set switches S6-S8 for the baud rate you will use. These switch settings are listed on the bottom of the HP E3472A/73A Emulator.

   The higher baud rates may not work reliably with all hosts and user interfaces. Make sure the baud rate you choose is supported by your host and user interface.

Example

To use a baud rate of 9600 baud, set the switches as follows:



To connect a serial cable

Connect an RS-232C modem cable from the host computer to the HP E3472A/73A Emulator. The recommended cable is HP part number C2932A. This is a 9-pin cable with one-to-one pin connections.

Caution

Use the recommended cable. If the cable is not shielded, or if the cable is not grounded at the serial controller, the HP E3472A/73A Emulator may be damaged by electrostatic discharge.

To verify serial communications

1. **Start a terminal emulator program on the host computer.**

   If you are using a PC, the Terminal application (HyperTerminal) in Microsoft Windows 95 will work fine.

   If you are using a UNIX workstation, you can use a terminal emulator such as kermit.

2. **Plug the power cord into the HP E3472A/73A Emulator.**

   When the HP E3472A/73A Emulator powers up, it sends a message (similar to the one that follows) to the serial port and then displays a prompt:

```
                  Copyright (c) Hewlett-Packard Co. 1987
All Rights Reserved.  Reproduction, adaptation, or translation without prior
written permission is prohibited, except as allowed under copyright laws.

  HPE3499B Series Emulation System
    Version:   A.07.00 17Aug96
    Location:  Generics

 HPE3472A Hitachi SH7040 Series Emulator
   Version:   A.00.00 17Aug96 17:07
   Speed:     33.3 MHz
   Memory:    0 KBytes
   PC Board:  f200-00e0-0000-78ff

R>
```

   The version numbers may be different for your HP E3472A/73A Emulator.

3. **Press the Return or Enter key a few times.**

   You should see a prompt such as "R>", "p>" or "c>".

See Also

"Problems with the Serial Interface" in Chapter 10.

Note

5

Connecting to the Target System

Connecting to a Target System

Attach the QFP socket/adapter to the target system in advance.

The HP E3472A/73A Emulator is connected to the target system by inserting the QFP cable attached to the emulation probe into the QFP socket/adapter.

QFP cable

Use one of the following QFP cables to connect the HP E3472A/73A Emulator to the target system.

- 112-pin QFP cable (HP Part Number E3472B)
- 144-pin QFP cable (HP Part Number E3472C)
- 168-pin QFP cable (HP Part Number E3473B)

QFP socket/adapter

The cables listed above come with a socket/adapter required for connecting to the target system.

When mounting and securing the processor to the target system, a socket cover is necessary.

The 112-pin cable comes with a socket cover. For 144- and 168-pin cables, you need to purchase it separately:

- 144-pin socket cover (HP Part Number E3472-61631)
- 168-pin socket cover (HP Part Number E3473-61630)

Connecting the HP E3472A/73A Emulator to the target system

Caution

To prevent the emulator and the target system from being damaged, be sure to follow the cautions below when handling them.

- Be sure to turn off the emulator and the target system before connecting them.
- Check that the orientation of the QFP socket/adapter and the QFP cable is correct.
- To prevent the emulator from being damaged by static electricity, store and use the emulator in a place resistant to static electricity.
- Check that the ground line of the emulator and that of the target system are properly connected.
- When turning the system on, switch on the target system first and then the emulator. When turning the system off, switch off the emulator first and then the target system.
- When supplying power to the emulator, check that the emulation probe is plugged into the target system or demo board.

Caution

Do not apply excessive force to the QFP cable. Doing so may damage the cable.

1 Check that the emulator and the target system are OFF.
2 Remove the processor from the target system.
3 Connect the QFP cable to the emulation probe.
4 Connect the QFP cable so that pin 1 of the QFP cable is inserted into pin 1 of the QFP socket/adapter on the target system (see Figure 5-1).
5 Switch on the target system; then switch on the emulator.

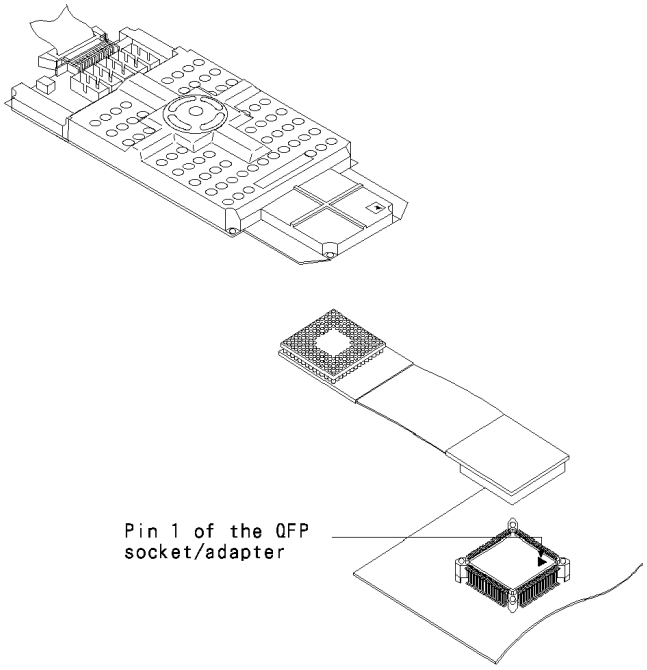


Figure 5-1. Connecting HP E3472A/73A Emulator into the Target System.

Note

6

Designing a Target System

Designing a Target System

This chapter will help you design a target system that will work with the HP E3472A/73A Emulator and describe instructions for use of the target system.

QFP socket/adapter

The following list shows available QFP socket/adapters.

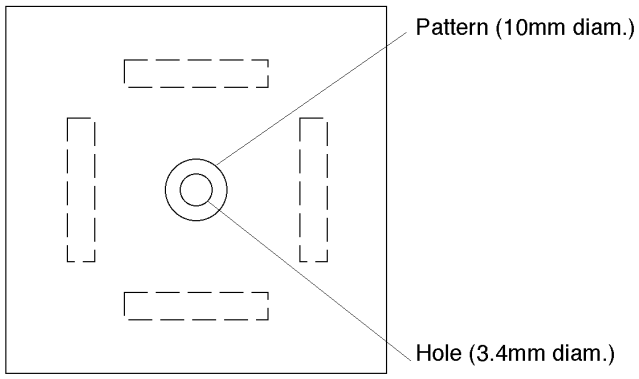
112 pins HP Part Number E3472-61620 (with socket cover)

144 pins HP Part Number E3472-61621

168 pins HP Part Number E3473-61620

To mount the QFP socket/adapter, solder it directly onto the target system board.

To mount the 168-pin QFP socket/adapter, bore a 3.4-mmϕ hole in the target system board so that the hole is located at the center of the bottom of the socket/adapter when mounted and make a 3-mm width pattern around the hole (see the figure below).



Target System Board (Bottom View)

Pin relationship between 177-pin connector and QFP socket/adapter

For pin assignment of the 177-pin connector for each of the 112-, 144-, and 168-pin QFP socket adapter, see Chapter 9 "Specifications and Characteristics."

Target interface

For electrical characteristics of the interface with the target system, see Chapter 9 "Specifications and Characteristics."

Cautions in designing target systems

You should remember the followings when designing target systems.

- For operating frequency and operating supply voltage:

  Supported range for the processor operation is 4.0 to 33.3 MHz in frequency and 5±0.25V in power. Processors that operate at 3.3 V are not supported.

7

Using the Logic Analyzer

Using the Logic Analyzer

This chapter describes you how to connect the logic analyzer to your emulator.

Connecting the Logic Analyzer

Follow the steps below to connect the logic analyzer to the HP E3472A/73A Emulator.

1. Disconnect the power source from the HP E3472A/73A Emulator
2. Switch off the target system.
3. Connect the logic analyzer to the host computer via a LAN.
   Enter the Configuration Screen of the logic analyzer to specify LAN parameters. See LAN User's Guide that comes with the logic analyzer for detail.

Note

If you specified the IP address for the logic analyzer when you installed HP B3755A/56A Debug User Interface, giving the same address will skip the addressing operation when you start the Debugger.

4. Connect the pods via the termination adaptors into the emulation probe.

   Connect the appropriate pods into the emulation probe according to the label ("POD 1", "POD 2", ..., "POD 5") on it. See Figure 7-1 and Table 7-1 to find the connection mapping for your logic analyzer.

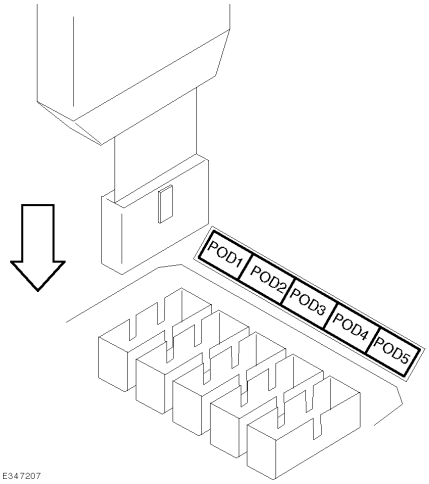


Figure 7-1. Connecting the Pod

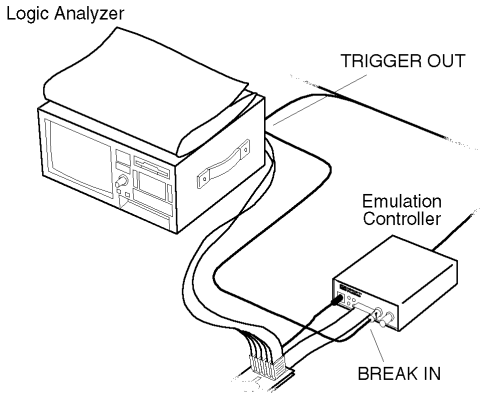
Table 7-1 Corespondance Emulation Probe with Pod

		Logic Analyzer		
		HP 16550, HP 1660/1, HP 1671	**HP 16554/5/6**	**HP 1670**
Emulation Probe	**POD 1**	Pod 1	Master Pod 1	Pod 1
	POD 2	Pod 2	Master Pod 2	Pod 2
	POD 3	Pod 3	Slave Pod 1	Pod 5
	POD 4	Pod 4	Slave Pod 2	Pod 6
	POD 5	Pod 5	Slave Pod 3	Pod 7

Note

- Be sure to use HP 01650-63203 for the termination adapters. None of the others can be used.
- Connect/disconnect the adapter with holding the connector side.

5 Connect the TRIGGER OUT terminal of the logic analyzer and the BREAK IN terminal of the emulation controller.



To verify the connection

Follow the steps below to verify the connection.

1. Power on the target system.
2. Connect the power source into the HP E3472A/73A Emulator.
3. Start the Debugger.

   Specify the IP address for the logic analyzer if necessary.
4. Use trace function to see tracing is properly performed with the logic analyzer.

Restrictions

Resource

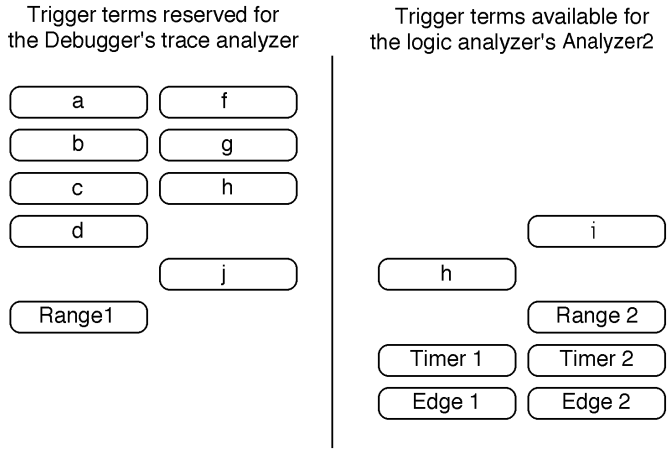
When you use the logic analyzer with HP E3472A/73A Emulator, the following resources are reserved for the Emulator upon the activation of the trace function.

Pod s Pods listed in Table 7-2 are reserved for the Emulator. The rest of the pods can be used for Analyzer2 (See the table below).

Table 7-2 Available Pods When Connected to the Emulator

	Logic Analyzer			
	HP 16550, HP 1661, HP 1671	**HP 1660**	**HP 16554/5/6**	**HP 1670**
Not Available	Pod 6	Pod 6	Expand Pod 4	Pod 8
Available for Analyzer2	None	Pod 7, Pod 8	Master Pod 3, Master Pod 4	Pod 3, Pod 4

Trigger Terms Trigger terms are partly reserved for the trace analyzer. The rest of the terms are available for Analyzer2, which can be configured as a timing analyzer or a state analyzer.



Trigger/Store Condition with the trace label "DATA" The data bus between the Emulator and the logic analyzer is 32 bit in width. The condition which determines the enable bits depends on the data bus width of the accessed area and the access size of the instruction. See the below.

8/16/32-bit data bus area	Same as the processor
Built-in ROM	32-bit data bus area
Peripheral registers and built-in RAM	32-bit data bus area (Long word access) 16-bit data bus area (Byte access and word access)

Mnemonics in the Trace List Normally, trace list shows the mnemonics for the instructions which were actually executed and does not show mnemonics for such instructions that were fetched but not executed.

However, mnemonics may not be displayed when the corresponding instruction was actually executed, or vice versa.

This can be observed around the bottom of the trace list and when the store condition is set.

Note

8

Specifications and Characteristics

Specifications and Characteristics

This chapter provides specifications and characteristics of HP E3472A/73A Emulator.

This chapter covers:

- Processor compatibility
- Supported logic analyzer
- Target system interface
- Electrical specification

Processor compatibility

The HP E3472A/73A Emulator supports the following Hitachi SH Series processors.

Table 8-1. Supported Processors (HP E3472A)

Processor	Package
SH7040	112-pin QFP
SH7041	144-pin QFP
SH7042	112-pin QFP
SH7043	144-pin QFP
SH7044	112-pin QFP
SH7045	144-pin QFP

Note SH7040 Series processors that operate at low voltage (3.3V) are not supported.

Table 8-2. Supported Processors (HP E3473A)

Processor	Package
SH7050	168-pin QFP
SH7051	168-pin QFP

Supported Logic Analyzers

Main frame [1]

16500B/C+16550A 102-channel logic analyzer card
16500B/C+16554A 68-channel logic analyzer card x 2
16500B/C+16555A/D 68-channel logic analyzer card x 2
16500B/C+16556A/D 68-channel logic analyzer card x 2

Portable

1660C/CS 136/102-channel portable logic analyzer [2]
1661C/CS 136/102-channel portable logic analyzer [2]
1670A/D 136/102-channel portable logic analyzer
1671A/D 136/102-channel portable logic analyzer

1 For 16500, a LAN card (16500H/L) is necessary.
2 LAN option is necessary.

Note Five pieces of the termination adapter (HP 01650-63203) are required to connect the HP E3472A/73A to the logic analyzer. You cannot use other termination adapters.

Target System Requirements

Connection to the target systems that operate at the following voltage and frequency is supported.

- The HP E3472A Emulator

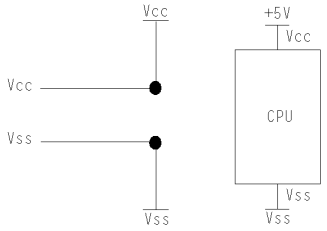
Operating voltage	5±0.25 V
Operating frequency	4.0 - 33.3 MHz

- The HP E3473A Emulator

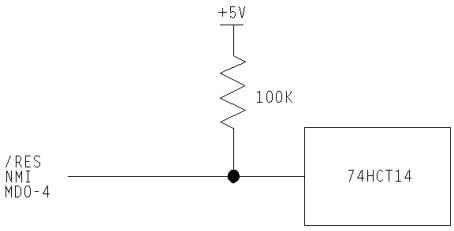
Operating voltage	5±0.25 V
Operating frequency	4.0 - 25.0 MHz

Target Interface (HP E3472A)

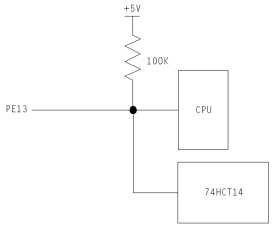
Vcc, Vss



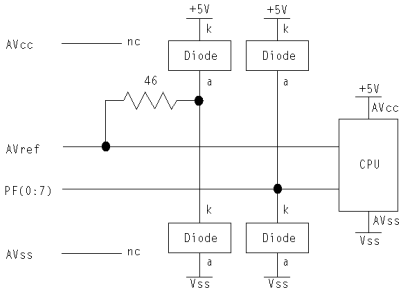
/RES, NMI, MD0 - 3



PE13



PF, AVcc, AVref, AVss

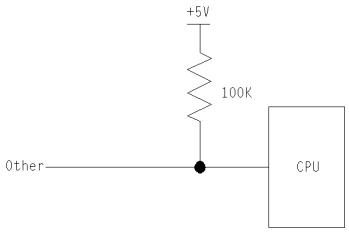


EXTAL, XTAL

Connect a circuit that meets the SH7040 Series specification.

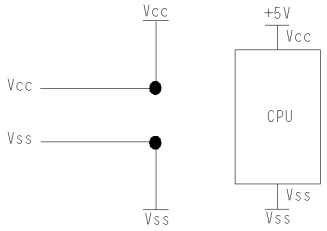
PLLVcc, PLLCAP, PLLVss

Others

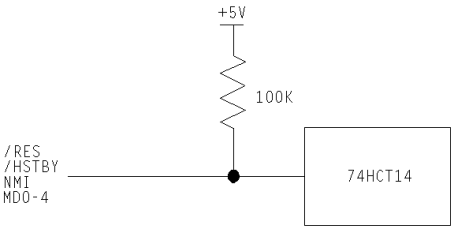


Target Interface (HP E3473A)

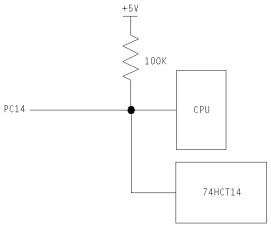
Vcc, Vss



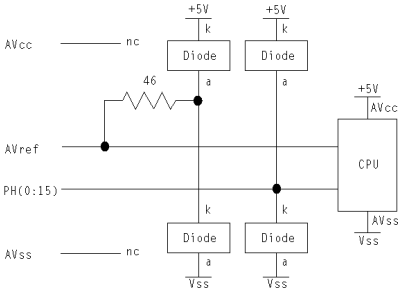
/RES, /HSTBY, NMI, MD0 - 3



PC14



PH, AVcc+, +AVre, AVss



Vpp, EXTAL, XTAL

Connect a circuit that meets the SH7050 Seriese specification.

PLLVcc, PLLCAP, PLLVss

Others

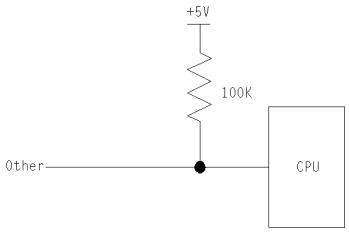


Table 8-3. E3472B PGA to QFP112 Adaptor Pin Assignment

PGA177 pin #	QFP112 pin #	Function name	PGA177 pin #	QFP112 pin #	Function name
1		nc	24	49	PA2
2		nc	25		nc
3		nc	26		nc
4	2	PE15	27	56	PD12
5	5	PC1	28		nc
6		nc	29	57	PD11
7	11	PC7	30	58	PD10
8		nc	31		nc
9	17	PC13	32	60	PD8
10	21	Vcc	33		nc
11		nc	34	65	V_{cc}
12		nc	35	68	PD2
13	28	PB5	36		nc
14		nc	37	73	MD3
15		nc	38	77	V_{cc}
16	29	PB6	39		nc
17	31	PB8	40	80	$PLLV_{cc}$
18	32	PB9	41		nc
19	35	WDTOVF	42	84	RES
20		nc	43	85	PE0
21	41	PA10	44	86	PE1
22	45	PA6	45		nc
23		nc	46	89	PE4

Table 8-3. E3472B PGA to QFP112 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP112 pin #	Function name	PGA177 pin #	QFP112 pin #	Function name
47		nc	69	30	PB7
48	93	PF2	70		nc
49	96	PF5	71	33	V_{ss}
50		nc	72		nc
51		nc	73	38	PA12
52		nc	74	42	PA9
53	104	PE6	75		nc
54	108	PE10	76	48	PA3
55	111	PE12	77	37	V_{cc}
56		nc	78	52	PD15
57	1	PE14	79	54	PD13
58		nc	80		nc
59	3	V_{ss}	81	59	PD9
60	6	PC2	82		nc
61	9	PC5	83	61	V_{ss}
62	12	PC8	84	63	PD6
63	15	PC11	85	66	PD4
64	18	PC14	86	69	PD1
65	22	PB1	87		nc
66	24	PB2	88	74	EXTAL
67	26	PB4	89		nc
68		nc	90		nc

Table 8-3. E3472B PGA to QFP112 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP112 pin #	Function name	PGA177 pin #	QFP112 pin #	Function name
91	81	PLLCAP	113	25	PB3
92	83	PA15	114	27	V_{ss}
93	87	PE2	115		nc
94	88	PE3	116	34	PA14
95		nc	117		nc
96	90	V_{ss}	118		nc
97	94	PF3	119	43	PA8
98	97	AV_{ss}	120	46	PA5
99		nc	121		nc
100	101	V_{ss}	122	50	PA1
101	102	PE5	123		nc
102	105	PE7	124	55	V_{ss}
103	109	V_{ss}	125		GND
104	112	PE13	126	62	PD7
105		GND	127		nc
106	4	PC0	128		nc
107	7	PC3	129		nc
108		nc	130	71	V_{ss}
109	13	PC9	131	75	MD2
110		nc	132		nc
111	19	PC15	133	78	MD1
112	23	V_{ss}	134	82	$PLLV_{ss}$

Table 8-3. E3472B PGA to QFP112 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP112 pin #	Function name	PGA177 pin #	QFP112 Pin #	Function name
135		nc	157	47	PA4
136		nc	158	39	V_{ss}
137	91	PF0	159	51	PA0
138	95	PF4	160	53	PD14
139	98	PF6	161		nc
140	100	AV_{cc}	162	64	PD5
141		nc	163	67	PD3
142		nc	164	70	PD0
143	106	PE8	165	72	XTAL
144	110	PE11	166	76	NMI
145		GND	167		nc
146	8	PC4	168	79	MD0
147	10	PC6	169		nc
148	14	PC10	170	92	PF1
149	16	PC12	171		nc
150	20	PB0	172	99	PF7
151		nc	173		nc
152		nc	174		Vnc
153		nc	175	103	V_{cc}
154	36	PA13	176	107	PE9
155	40	PA11	177		GND
156	44	PA7			

Table 8-4. E3472C PGA to QFP144 Adaptor Pin Assignment

PGA177 pin #	QFP144 pin #	Function name	PGA177 pin #	QFP144 pin #	Function name
1		nc	24	62	PA21
2	1	PA23	25	66	PD21
3	3	PA22	26		nc
4	5	PE15	27	72	PD16
5	8	PC1	28		nc
6	12	Vcc	29	73	PD15
7	16	PC7	30	74	PD14
8		nc	31	76	PD12
9	22	PC13	32	78	PD11
10	26	Vcc	33	81	PD9
11	30	PA19	34	85	V_{cc}
12		nc	35	89	PD2
13	36	PB5	36		nc
14		nc	37	95	MD3
15		nc	38	99	V_{cc}
16	37	PB6	39	101	PA17
17	39	PB8	40	104	PLLVcc
18	41	PB9	41		nc
19	44	WDTOVF	42	108	RES
20		nc	43	109	PE0
21	50	PA10	44	110	PE1
22	54	PA6	45	112	V_{cc}
23	58	PA27	46	114	PE4

Table 8-4. E3472C PGA to QFP144 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP144 pin #	Function name	PGA177 pin #	QFP144 pin #	Function name
47		nc	69	38	PB7
48	120	PF2	70	40	V_{cc}
49	123	PF5	71	42	V_{ss}
50		nc	72	45	PD31
51		nc	73	48	PA12
52	132	PA2	74	51	PA9
53	136	PA5	75	55	V_{ss}
54	140	PE10	76	59	PD26
55	143	PE12	77	63	V_{cc}
56		nc2	78	67	PD20
57	2	PE14	79	70	PD17
58	4	PA21	80		nc
59	6	V_{ss}	81	75	PD13
60	9	PC2	82	77	V_{cc}
61	13	PC5	83	79	V_{ss}
62	17	PC8	84	82	PD6
63	20	PC11	85	86	PD5
64	23	PC14	86	90	PD2
65	27	PB1	87		nc
66	31	PB2	88	96	EXTAL
67	34	PB4	89	100	PA16
68		nc	90		nc

Table 8-4. E3472C PGA to QFP144 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP144 pin #	Function name	PGA177 pin #	QFP144 pin #	Function name
91	105	PLLCAP	113	32	PB3
92	107	PA15	114	35	V_{ss}
93	111	PE2	115		nc
94	113	PE3	116	43	PA14
95	115	PE5	117	46	PD30
96	117	V_{ss}	118		nc
97	121	PF3	119	52	PA8
98	124	AV_{ss}	120	56	PA5
99		nc	121	60	PD25
100	129	V_{ss}	122	64	PD23
101	133	PA3	123	68	PD19
102	137	PE7	124	71	V_{ss}
103	141	V_{ss}	125		GND
104	144	PE13	126	80	PD10
105		GND	127	83	PD7
106	7	PC0	128	87	V_{ss}
107	10	PC3	129	91	PD1
108	14	V_{ss}	130	93	V_{ss}
109	18	PC9	131	97	MD2
110		nc	132		nc
111	24	PC15	133	102	MD1
112	28	V_{ss}	134	106	$PLLV_{ss}$

Table 8-4. E3472C PGA to QFP144 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP144 pin #	Function name	PGA177 pin #	QFP144 pin #	Function name
135		nc	157	57	PA28
136	116	PE6	158	61	V_{ss}
137	118	PF0	159	65	PD22
138	122	PF4	160	69	PD18
139	125	PF6	161		GND
140	127	AV_{cc}	162	84	PD6
141	130	PA0	163	88	PD4
142	134	PA4	164	92	PD0
143	138	PE8	165	94	XTAL
144	142	PE11	166	98	NMI
145		GND	167		nc
146	11	PC4	168	103	MD0
147	15	PC6	169		nc
148	19	PC10	170	119	PF1
149	21	PC12	171		nc
150	25	PB0	172	126	PF7
151	29	PA20	173	128	AV_{cc}
152	33	PA18	174	131	PA1
153		nc	175	135	V_{cc}
154	47	PA13	176	139	PE9
155	49	PA11	177		GND
156	53	PA7			

Table 8-5. E3473B PGA to QFP168 Adaptor Pin Assignment

PGA177 pin #	QFP168 pin #	Function name	PGA177 pin #	QFP168 pin #	Function name
1	1	PG9	24	71	PE4
2	2	PG10	25	75	PE7
3	4	PG12	26	79	V_{cc}
4	6	PG14	27	82	PE12
5	9	PB0	28	84	PE14
6	13	Vcc	29	85	PD0
7	17	PA0	30	86	PD1
8	21	Vcc	31	88	PD3
9	25	PA6	32	90	PD4
10	29	Vcc	33	93	PD6
11	33	PA12	34	97	V_{cc}
12	37	Vcc	35	101	PD12
13	40	PB7	36	105	V_{cc}
14	42	PB9	37	109	MD3
15	43	PB10	38	113	V_{cc}
16	44	PB11	39	117	PF3
17	46	PC1	40	121	$PLLV_{cc}$
18	48	PC2	41	124	HSTBY
19	51	WDTOVF	42	126	RES
20	55	V_{cc}	43	127	PF4
21	59	PC9	44	128	PF5
22	63	PC13	45	130	V_{cc}
23	67	PE1	46	132	PF8

Table 8-5. E3473B PGA to QFP168 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP168 pin #	Function name	PGA177 pin #	QFP168 pin #	Function name
47	135	PF11	69	45	PC0
48	139	PH2	70	47	V_{cc}
49	143	PH5	71	49	V_{ss}
50	147	PH8	72	52	PC4
51	151	PH10	73	56	PC7
52	155	PH13	74	60	PC10
53	159	PG0	75	64	V_{ss}
54	163	PG4	76	68	PE2
55	166	PG6	77	72	V_{cc}
56	168	PG8	78	76	PE8
57	3	PG11	79	80	PE11
58	5	PG13	80	83	PE13
59	7	V_{ss}	81	87	PD2
60	10	PB1	82	89	V_{cc}
61	14	PB4	83	91	V_{ss}
62	18	PA1	84	94	PD7
63	22	PA4	85	98	PD10
64	26	PA7	86	102	PD13
65	30	PA10	87	106	PF0
66	34	PA13	88	110	EXTAL
67	38	PB6	89	114	PF1
68	41	PB8	90	118	V_{pp}

Table 8-5. E3473B PGA to QFP168 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP168 pin #	Function name	PGA177 pin #	QFP168 pin #	Function name
91	122	PLLCAP	113	35	PA14
92	125	CK	114	39	V_{ss}
93	129	PF6	115		nc
94	131	PF7	116	50	PC3
95	133	PF9	117	53	PC5
96	136	V_{ss}	118	57	V_{ss}
97	140	PH3	119	61	PC11
98	144	AV_{ss}	120	65	PC14
99	148	PH9	121	69	PE3
100	152	AV_{ss}	122	73	PE5
101	156	PH14	123	77	PE9
102	160	PG1	124	81	V_{ss}
103	164	V_{ss}	125		GND
104	167	PG7	126	92	PD5
105		GND	127	95	PD8
106	8	PG15	128	99	V_{ss}
107	11	PB2	129	103	PD14
108	15	V_{ss}	130	107	V_{ss}
109	19	PA2	131	111	MD2
110	23	V_{ss}	132	115	V_{ss}
111	27	PA8	133	119	MD1
112	31	V_{ss}	134	123	$PLLV_{ss}$

Table 8-5. E3473B PGA to QFP168 Adaptor Pin Assignment (Continued)

PGA177 pin #	QFP168 pin #	Function name	PGA177 pin #	QFP168 pin #	Function name
125		nc	157	66	PE0
136	134	PF10	158	70	V_{ss}
137	137	PH0	159	74	PE6
138	141	PH4	160	78	PE10
139	145	PH6	161		GND
140	149	AV_{ref}	162	96	PD9
141	153	PH11	163	100	PD11
142	157	PH15	164	104	PD15
143	161	PG2	165	108	XTAL
144	165	PG5	166	112	NMI
145		GND	167	116	PF2
146	12	PB3	168	120	MD0
147	16	PB5	169		nc
148	20	PA3	170	138	PH1
149	24	PA5	171	142	AV_{cc}
150	28	PA9	172	146	PH7
151	32	PA11	173	150	AV_{cc}
152	36	PA15	174	154	PH12
153		nc	175	158	V_{cc}
154	54	PC6	176	162	PG3
155	58	PC8	177		GND
156	62	PC12			

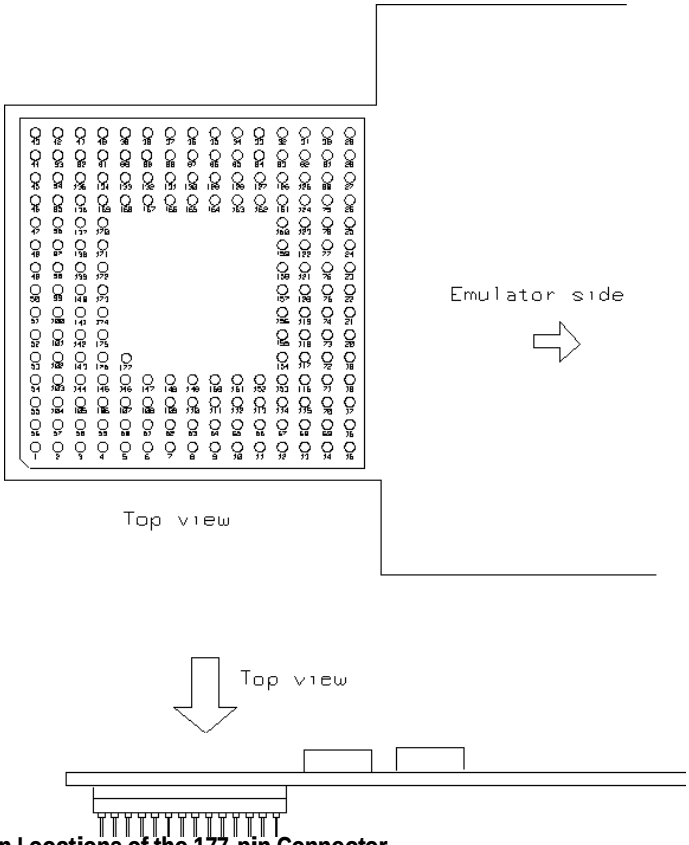


Figure 8-1. Pin Locations of the 177-pin Connector

Electrical Specifications

BNC, labeled TRIGGER OUT

Output Drive Logic high level >= 2.0 V when occurring monitor program with 50-ohm load or when in reset. Logic low level <= 0.4 V when running user code with 50-ohm load.

BNC, labeled TRIGGER IN

Input Edge-triggered TTL level input (positive high), 20 pf, with 2K ohms to ground in parallel. Maximum input: 5 V above $V_{CC;}$ 5 V below ground.

Communications

Seria l Port 9-pin female type "D" subminiature connector. RS-232 DCE to 115.2 kbaud.

10BASE-T LAN Port RJ-45 connector. IEEE 802.3 10BASE-T (StarLAN).

10BASE2 LAN Port 50-ohm BNC connector. IEEE 802.3 10BASE2 (ThinLAN). When using this connector, the HP E3472A/73A Emulator provides the functional equivalent of a Medium Attachment Unit (MAU) for ThinLAN.

Power Supply

Input 100-240Vac, 1.0Amax, 50/60Hz.

Output 12Vdc, 3.3A

Table 8-6. Clock Timing (E3472A)

Characteristic	Symbol	SH7040		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
Operating frequency	f_{op}	4	28.7	4	33.3	4	33.3	MHz
Clock cycle time	t_{cyc}	34.8	250	30	250	30	250	ns
Clock low-pulse width	t_{CL}	10	-	13	-	7	-	ns
Clock high-pulse width	t_{CH}	10	-	15	-	7	-	ns
Clock rise time	t_{cr}	-	5	-	4	-	8	ns
Clock fall time	t_{cf}	-	5	-	3	-	8	ns
EXTAL input frequency	t_{EX}	4	10	4	10	4	10	MHz
EXTAL input cycle time	t_{Excyc}	100	250	100	250	100	250	ns
EXTAL input low-level pulse width	t_{EXL}	40	-	40	-	40	-	ns
EXTAL input high-level pulse width	t_{EXH}	40	-	40	-	40	-	ns
EXTAL input rise time	t_{EXR}	-	5	-	5	-	5	ns
EXTAL input fall time	t_{EXF}	-	5	-	5	-	5	ns
Reset Oscillation setting time	t_{OSC1}	10	-	10	-	10	-	ms
Software standby oscillation setting time	t_{OSC2}	10	-	10	-	10	-	ms

*1 Typical outputs measured with 50pF load

Table 8-7. Control Signal Timing (E3472A)

Characteristic	Symbol	SH7040		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
RES rise time	t_{RESr}	-	200			-	200	ns
RES fall time	t_{RESf}	-	200			-	200	ns
RESET pulse width	t_{RESW}	20	-			20	-	t_{cyc}
MRESET pulse width	t_{MRESW}	20	-			20	-	t_{cyc}
NMI rise time	t_{NMIr}	-	200			-	200	ns
NMI fall time	t_{NMIf}	-	200			-	200	ns
RES setup time	t_{RESS}	35	-			85	-	ns
MRES setup time	t_{MRESS}	35	-			45	-	ns
NMI setup time	t_{NMIS}	35	-			95	-	ns
$\overline{IRQ0}$ - $\overline{IRQ7}$ setup time (edge detection time)	t_{IRQES}	35	-			45	-	ns
$\overline{IRQ0}$ - $\overline{IRQ7}$ setup time (level detection time)	t_{IRQLS}	35	-			45	-	ns
NMI hold time	t_{NMIH}	35	-			35	-	ns
$\overline{IRQ0}$ - $\overline{IRQ7}$ hold time	t_{IRQEH}	35	-			35	-	ns
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	-	35			-	40	ns
Bus request setup time	t_{BRQS}	35	-			45	-	ns
Bus acknowledge delay time 1	t_{BACD1}	-	35			-	40	ns
Bus acknowledge delay time 2	t_{BACD2}	-	35			-	40	ns
Bus 3-state delay time	t_{BZD}	-	35			-	40	ns

*1 Typical outputs measured with 50pF load

Table 8-8. Bus Timing (E3472A)

Characteristic	Symbol	SH7040		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
Address delay time	t_{AD}	(2)	18	-	9	-	23	ns
$\overline{CS}$ delay time 1	t_{CSD1}	(2)	21	-	11	-	26	ns
$\overline{CS}$ delay time 2	t_{CSD2}	(2)	21	-	8	-	26	ns
Read strobe delay time 1	t_{RSD1}	(2)	18	-	9	-	23	ns
Read strobe delay time 2	t_{RSD2}	(2)	18	-	7	-	23	ns
Read data setup time	t_{RDS}	(15)	-	15	-	25	-	ns
Read data hold time	t_{RDH}	0	-	0	-	0	-	ns
Write strobe delay time 1	t_{WSD1}	(2)	18	-	11	-	23	ns
Write strobe delay time 2	t_{WSD2}	(2)	18	-	8	-	23	ns
Write data delay time	t_{WDD}	-	35	-	14	-	40	ns
Write data hold time	t_{WDH}	0	(10)	4	-	-5	-	ns
Wait setup time	t_{WTS}	15	-	15	-	25	-	ns
Wait hold time	t_{WTH}	0	-	0	-	0	-	ns
$\overline{RAS}$ delay time 1	t_{RASD1}	(2)	18	-	10	-	23	ns
$\overline{RAS}$ delay time 2	t_{RASD2}	(2)	18	-	7	-	23	ns
$\overline{CAS}$ delay time 1	t_{CASD1}	(2)	18	-	8	-	23	ns
$\overline{CAS}$ delay time 2	t_{CASD2}	(2)	18	-	6	-	23	ns
Read data access time	t_{ACC}	39.6	-	39.6	-	29.6	-	ns
RD to read data access time	t_{OE}	22.2	-	22.2	-	12.2	-	ns
Column address to read data access time	t_{AA}	39.6	-	39.6	-	29.6	-	ns
$\overline{RAS}$ to read data access time	t_{RAC}	57	-	57	-	47	-	ns
$\overline{CAS}$ to read data access time	t_{CAC}	4.8	-	4.8	-	-5.2	-	ns
Low address hold time	t_{RAH}	2.4	-	12	-	-2.6	-	ns
Low address setup time	t_{ASR}	-.1	-	12	-	-5.1	-	ns

*1 Typical outputs measured with 50pF load

Table 8-8. Bus Timing (E3472A)
(Continued)

Characteristic	Symbol	SH7040		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
Data input setup time	t_{DS}	-7.6	-	8	-	-12.6	-	ns
Data input hold time	t_{DH}	20	-	50	-	15	-	ns
Write address setup time	t_{AS}	0	-	14	-	-5	-	ns
Write address hold time	t_{WR}	5	-	14	-	0	-	ns
Write data hold time	t_{WRH}	0	-	7	-	-5	-	ns
RDWR delay time 1	t_{RWD1}	(2)	18	-	9	-	23	ns
RDWR delay time 2	t_{RWD2}	(2)	18	-	7	-	23	ns
High-speed page mode $\overline{CAS}$ precharge time	t_{CP}	9.8	-	35	-	6.8	-	ns
$\overline{RAS}$ precharge time	t_{RP}	37.2	-	52	-	34.2	-	ns
$\overline{CAS}$ setup time	t_{CSR}	10	-	49	-	5	-	ns
AH delay time 1	t_{AHD1}	(2)	18	-	10	-	23	ns
AH delay time 2	t_{AHD2}	(2)	18	-	10	-	23	ns
Multiplexed address delay time	t_{MAD}	(2)	18	-	14	-	23	ns
Multiplexed address hold time	t_{MAH}	0	-	18	-	-5	-	ns
DACK0-DACK1 delay time 1	t_{DACKD1}	(2)	21	(omitted)		-	26	ns

*1 Typical outputs measured with 50pF load

Table 8-9. DMAC Timing (E3472A)

Characteristic	Symbol	SH7040		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
DREQ0	DREQ1 setup time	t_{DRQS}	18	-			28	-
DREQ0	DREQ1 hold time	t_{DRQH}	18	-			18	-
DREQ0	DREQ1 pulse width	t_{DRQW}	1.5	-			1.5	-
DRAK output delay time	t_{DRAKD}	-	18			-	23	ns

*1 Typical outputs measured with 50pF load

Table 8-9. Clock Timing (E3473A)

Characteristic	Symbol	SH7050		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
Operating frequency	f_{op}	TBD	20	4	25	TBD	25	MHz
Clock cycle time	t_{cyc}	50	TBD	50	250	50	TBD	ns
Clock low-pulse width	t_{CL}	20	-	19	-	17	-	ns
Clock high-pulse width	t_{CH}	20	-	24	-	17	-	ns
Clock rise time	t_{cr}	-	5	-	3	-	8	ns
Clock fall time	t_{cf}	-	5	-	2	-	8	ns
EXTAL input frequency	t_{EX}	TBD	10	4	10	TBD	10	MHz
EXTAL input cycle time	t_{Excyc}	100	TBD	100	250	100	TBD	ns
EXTAL input low-level pulse width	t_{EXL}	TBD	-	40	-	TBD	-	ns
EXTAL input high-level pulse width	t_{EXH}	TBD	-	40	-	TBD	-	ns
EXTAL input rise time	t_{EXR}	-	TBD	-	5	-	TBD	ns
EXTAL input fall time	t_{EXF}	-	TBD	-	5	-	TBD	ns
Reset Oscillation setting time	t_{OSC1}	10	-	10	-	10	-	ms
Software standby oscillation setting time	t_{OSC2}	10	-	10	-	10	-	ms

*1 Typical outputs measured with 50pF load

Table 8-10. Clock Signal Timing (E3473A)

Characteristic	Symbol	SH7050		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
RES rise time	t_{RESr}	-	200			-	200	ns
RES fall time	t_{RESf}	-	200			-	200	ns
RESET pulse width	t_{RESW}	20	-			20	-	t_{cyc}
MRESET pulse width	t_{MRESW}	TBD	-			TBD	-	t_{cyc}
NMI rise time	t_{NMIr}	-	200			-	200	ns
NMI fall time	t_{NMIf}	-	200			-	200	ns
RES setup time	t_{RESS}	30	-			80	-	ns
MRES setup time	t_{MRESS}	TBD	-			TBD+10	-	ns
NMI setup time	t_{NMIS}	30	-			90	-	ns
$\overline{IRQ0}$ - $\overline{IRQ7}$ setup time (edge detection time)	t_{IRQES}	30	-			40	-	ns
$\overline{IRQ0}$ - $\overline{IRQ7}$ setup time (level detection time)	t_{IRQLS}	30	-			40	-	ns
NMI hold time	t_{NMIH}	TBD	-			TBD	-	ns
$\overline{IRQ0}$ - $\overline{IRQ7}$ hold time	t_{IRQEH}	TBD	-			TBD	-	ns
$\overline{IRQOUT}$ output delay time	t_{IRQOD}	-	25			-	30	ns
Bus request setup time	t_{BRQS}	TBD	-			TBD+10	-	ns
Bus acknowledge delay time 1	t_{BACD1}	-	TBD			-	TBD+5	ns
Bus acknowledge delay time 2	t_{BACD2}	-	TBD			-	TBD+5	ns
Bus 3-state delay time	t_{BZD}	-	TBD			-	TBD+5	ns

*1 Typical outputs measured with 50pF load

Table 8-11. Bus Timing (E3473A)

Characteristic	Symbol	SH7050		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
Address delay time	t_{AD}	(TBD)	25	-	12	-	30	ns
$\overline{CS}$ delay time 1	t_{CSD1}	-	30	-	11	-	35	ns
$\overline{CS}$ delay time 2	t_{CSD2}	-	30	-	7	-	35	ns
Read strobe delay time 1	t_{RSD1}	-	25	-	12	-	30	ns
Read strobe delay time 2	t_{RSD2}	-	25	-	10	-	30	ns
Read data setup time	t_{RDS}	(15)	-	15	-	25	-	ns
Read data hold time	t_{RDH}	0	-	0	-	0	-	ns
Write strobe delay time 1	t_{WSD1}	(TBD)	25	-	11	-	30	ns
Write strobe delay time 2	t_{WSD2}	(TBD)	25	-	7	-	30	ns
Write data delay time	t_{WDD}	-	40	-	12	-	45	ns
Write data hold time	t_{WDH}	0	-	5	-	-5	-	ns
Wait setup time	t_{WTS}	15	-	15	-	25	-	ns
Wait hold time	t_{WTH}	10	-	10	-	10	-	ns
Read data access time	t_{ACC}	65	-	65	-	55	-	ns
RD to read data access time	t_{OE}	40	-	40	-	30	-	ns
DACK0-DACK1 delay time 1	t_{DACKD1}	-	30	(omitted)		-	35	ns

*1 Typical outputs measured with 50pF load

Table 8-12. DMAC Timing (E3473A)

Characteristic	Symbol	SH7050		Typical (*1)		Worst Case		Unit
		min	max	min	max	min	max	
DREQ0	DREQ1 setup time	t_{DRQS}	27	-			37	-
DREQ0	DREQ1 hold time	t_{DRQH}	30	-			30	-
DREQ0	DREQ1 pulse width	t_{DRQW}	1.5	-			1.5	-
DRAK output delay time	t_{DRAKD}	-	25			-	30	ns

*1 Typical outputs measured with 50pF load

Environmental Specifications

Temperature

Operating, 0 to +40 °C (+32 to +104 °F); non-operating, -40 to +60 °C (-40 to +140 °F).

Altitude

Operating, 0 to 2,000 m (6,500ft); non-operating, 4,600 m (15,000 ft).

Relative Humidity

15% to 95% (@40 °C).

Regulatory Compliance

This product complies with the requirements of the Low Voltage Directive 73/23/EEC and the EMC Directive 89/336/EEC, and conforms to the following specifications:

Electromagnetic Compatibility

CISPR 11:1990 / EN 55011:1991	Group 1, Class A
IEC 1000-3-3:1994 / EN 61000-3-3:1995	
IEC 801-2:1991 / EN 50082-1:1992	4 kV CD, 8 kV AD
IEC 801-3:1984 / EN 50082-1:1992	3 V/m, {1kHz 80% AM, 27-1000 MHz}
IEC 801-4:1988 / EN 50082-1:1992	0.5 kV Signal Lines, 1 kV Power Lines

Safety

IEC 1010-1(1990) + Amendment 1(1992)

CSA-C22.2 No.1010.1 - 92

Note

9

Updating Firmware

Updating Firmware

You can update the firmware in the HP E3472A/73A Emulator by running the **progflash** utility program. **progflash** downloads code from files on the host computer into Flash EPROM memory which is built-in to the HP E3472A/73A Emulator.

This chapter describes how to:

- Components of the software updates.
- Update firmware with the "**progflash**" command.
- Display current firmware version information.

Components of the software updates

If you're using the HP E3472A/73A Emulator with an HP 9000/700 computer or a Sun SPARCsystem computer:

The HP E3755A/56A Debug User Interface contains the **progflash program and flashware for the HP E3472A/73A Emulator.**

If you're using an IBM PC AT compatible computer:

The HP 64700 SW Update Utility product included in the HP E3755A/56A Debug User Interface contains the **progflash program and flashware for the HP E3472A/73A Emulator.**

Setting up the Host Software

Before you can use **progflash** command, you may need to configure some communication parameters:

- If you will be using on a workstation, you have to set up the 64700tab.net file. After setting up, you can use **progflash** command via a LAN.
- If you will be using on a PC, you have to set up the 64700tab file and connect your PC to the Emulator with an RS-232 cable.

To set up the 64700tab.net file

When you use the HP E3472A/73A Emulator on a workstation and want to update firmware using **progflash** command, you need to set up 64700tab.net file to specify the destination Emulator.

1. Make up a *logical name* for the HP E3472A/73A Emulator.

   You will use this name to identify the HP E3472A/73A Emulator. This name can be same as in /etc/hosts file.

2. Find the IP address of the HP E3472A/73A Emulator.
3. Edit the **/usr/hp64000/etc/64700tab.net** file and add one line with the following format:

   ```
   lan: <logical_name> <processor_type> <connection_info>
   ```

<logical_name> The logical name. This name is to identify the Emulator.

<processor_type> A general classification of the processor type. For the HP E3472A/73A Emulator, the processor_type is "*".

<connection_info> The IP address of the HP E3472A/73A Emulator.

The 64700tab.net file is located in the directory $HP64000/etc (/usr/hp64000/etc by default).

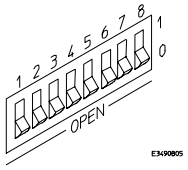
To set up the 64700tab file

1 Add following one line to \hp64700\tables\64700tab file.
In this case, <logical_name> is **emul_com1** and the baud rate is set to 9600.

```
emul_com1 unknown COM1 OFF 9600 NONE ON 1 8
```

Example

To use a baud rate of 9600 baud, set the switches as follows:



To update firmware with "**progflash**"

1. In the case of a workstation, make sure your HP E3472A/73A Emulator is listed in the 64700tab.net file.
2. In the case of a PC, make sure your HP E3472A/73A Emulator is listed in the 64700tab file.
3. Install the update software on your computer.

   The following table describes the files that are used when updating firmware.

Files Used During Firmware Updates

File	Description	Location on HP 9000 or Sun SPARCsystem computers	Location on IBM PC AT compatible computers
progflash	Executable program.	$HP64000/bin	\hp64700\bin
<product>.cfg <product>.X	Product configuration file. Product code file.	$HP64000/inst/update	\hp64700\update

4. Enter the **progflash** command.
5. Answer the questions asked by the **progflash** command.

   The **progflash** command downloads code from files on the host computer into Flash EPROM memory in the HP E3472A/73A Emulator.

   Instead of running progflash interactively, you may use options to the progflash command:

   ```
   progflash [-v] [emul_name] [products_to_update ...]
   ```

   The **-v** option means "verbose". It causes progress status messages to be displayed during operation.

   The **emul_name** option is the logical emulator name as specified in the 64700tab or 64700tab.net file.

   The **products_to_update** option names the products whose firmware is to be updated. For the HP E3472A/73A Emulator, the product name is "E3472".

   If you enter the **progflash** command without options, it becomes interactive. If you don't include the **emul_name** option, it displays the logical names in the 64700tab or 64700tab.net file and asks you to choose one. If you don't include the **products_to_update** option, it displays the products which have firmware update files on the system and asks you to

choose one. (In the interactive mode, only one product at a time can be updated.) You can abort the interactive **progflash** command by pressing <CTRL>c.

progflash will print "Flash programming SUCCEEDED" and return 0 if it is successful; otherwise, it will print "Flash programming FAILED" and return a nonzero (error).

You can verify the update by displaying the firmware version information.

Example

To update the firmware in "myprobe", you could enter the following command:

```
progflash -v myprobe E3472
```

To display current firmware version information

- Use **telnet** or a terminal emulator to access the built-in "terminal interface" and use the **ver** command to view the version information for firmware currently in the HP E3472A/73A Emulator.

If the firmware doesn't appear to be updated

Though Flash EPROM is very reliable, it can fail. If the HP E3472A/73A Emulator determines the Flash EPROM is not working, it will try to use the boot code in its Flash EPROMs. The only useful operation the boot code allows is running **progflash**.

☐ Make sure the current version information is incorrect by comparing it with the version numbers of the update software.

☐ Try updating the firmware again.

If none of these steps solves the problem, contact your local HP Representative.

If there is a power failure during a firmware update

If there is a power glitch during a firmware update, some bits may be lost during the download process, possibly resulting in an HP E3472A/73A Emulator that will not boot up.

☐ Set switch S4 to OPEN, then cycle power. This tells the HP E3472A/73A Emulator to ignore everything in the Flash EPROM except the boot code.

☐ Repeat the firmware update process.

☐ Set switch S4 to CLOSED, then cycle power. This restores the HP E3472A/73A Emulator to its normal mode.

See Also

"If the data in ROM is corrupt" in Chapter 10.

10

Solving Problems

Solving Problems

If you have problems with the HP E3472A/73A Emulation Probe System, your first task is to determine the source of the problem. Problems may originate in any of the following places:

- The HP E3472A/73A Emulator itself
  - Emulation controller
  - Emulation probe
  - 50-pin ribbon cable
- The connection between the HP E3472A/73A Emulator and your host computer
- The interface software on the host computer
- The connection between the HP E3472A/73A Emulator and the target system
- The target system

You can use several means to determine the source of the problem:

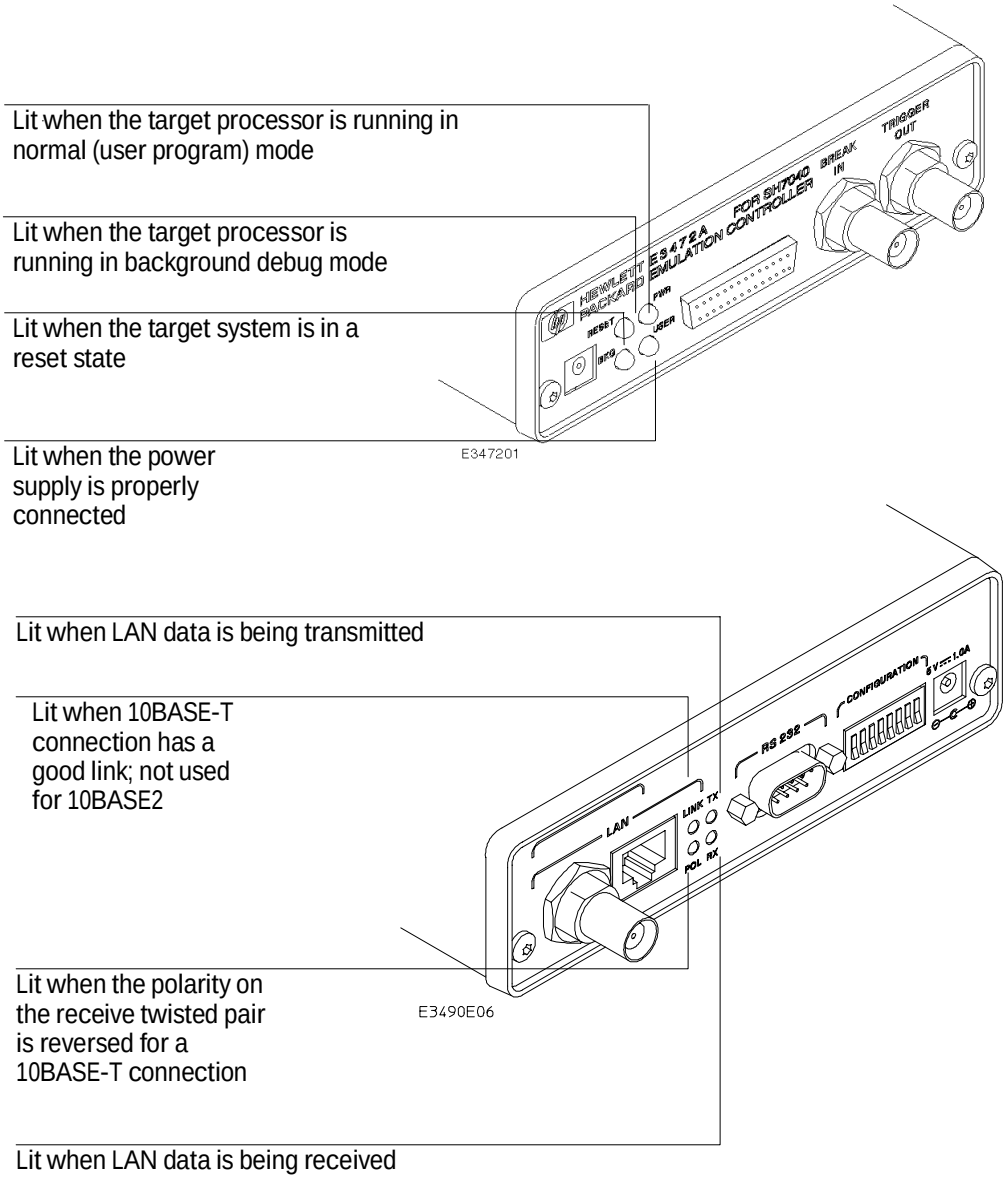
- The status lights on the emulation controller
- Error messages displayed on the host computer
- Diagnostic tests performed using the host computer
- HP E3472A/73A Emulator "performance verification" tests

You can run these tests for each of the emulation controller and emulation probe.

Status Lights

The HP E3472A/73A Emulator communicates various modes and error conditions via the status lights.

The following illustration shows the status lights on both sides of the HP E3472A/73A Emulator and what they mean:


Lit when the target processor is running in normal (user program) mode
Lit when the target processor is running in background debug mode
Lit when the target system is in a reset state
Lit when the power supply is properly connected
HEWLETT PACKARD
E5472A
EMULATION CONTROLLER
FOR SH7040
BREAK IN
TRIGGER OUT
RESET
INTG
PWR
USER
E347201
Lit when LAN data is being transmitted
Lit when 10BASE-T connection has a good link; not used for 10BASE2
Lit when the polarity on the receive twisted pair is reversed for a 10BASE-T connection
Lit when LAN data is being received
LAN
LINK TX
POL RX
RS 232
CONFIGURATION
E3490E06

Problems with the LAN Interface

If you cannot verify LAN communication

Use the "telnet" command on the host computer to verify LAN communication. After powering up the HP E3472A/73A Emulator, it takes up to a minute before the HP E3472A/73A Emulator can be recognized on the network. After a minute, try the "telnet <internet address>" command.

If "telnet" does not make the connection:

- ☐ Make sure that you have connected the HP E3472A/73A Emulator to the proper power source and that the power light is lit.
- ☐ Make sure that the LAN cable is connected. Refer to your LAN documentation for testing connectivity.
- ☐ Make sure that only one of the LAN ports is connected.
- ☐ Make sure the HP E3472A/73A Emulator communication configuration switches are set correctly. Unplug the HP E3472A/73A Emulator power cord, then plug it in again to make sure the switch settings are read correctly by the HP E3472A/73A Emulator.
- ☐ Make sure that the HP E3472A/73A Emulator's IP address is set up correctly. Use the RS-232 port to verify this that the IP address is set up correctly. When you are connected to the RS-232 port, run performance verification on the HP E3472A/73A Emulator's LAN interface with the "pv" command.

If "telnet" makes the connection, but no prompt (for example, R>, M>, U>, etc.) is supplied:

- It's possible that the host software is in the process of running a command. You can use <CTRL>c to interrupt and get the Terminal Interface prompt.
- It's also possible for there to be a problem with the HP E3472A/73A Emulator firmware while the LAN interface is still up and running. In this case, you must reboot the HP E3472A/73A Emulator by disconnecting power to the HP E3472A/73A Emulator and reconnecting it again.

If you have LAN connection problems

- Try to "ping" the HP E3472A/73A Emulator. At your operating system prompt, type:

  ```
  ping <hostname or IP address>
  ```

  If it does not respond:

  1. Check that switch S1 is "0" (attached to LAN, not RS-232).

  2. Check that switch S5 is in the correct position for your LAN interface (either 10BASE2 or 10BASE-T).

  (Remember: if you change any switch settings, the changes do not take effect until you cycle power.)

- If the HP E3472A/73A Emulator still does not respond to a "ping", you need to verify the IP address and gateway mask of the HP E3472A/73A Emulator. To do this, connect the HP E3472A/73A Emulator to a terminal or terminal emulator (see page 34), change the switch settings so it is connected to RS-232, and enter the "lan" command. The output looks something like this:

  ```
  lan -i 15.5.24.116
  lan -g 15.5.23.1
  lan -p 6470
  Ethernet Address : 08000909BAC1
  ```

  "lan -i" shows the internet address is 15.5.24.116 in this case. If the Internet address (IP) is not what you expect, you can change it with the 'lan -i <new IP>' command.

"lan -g" shows the gateway address. Make sure it is the address of your gateway if you are connecting from another subnet, 0.0.0.0 if you are connecting from the local subnet.

"lan -p" shows the port is 6470. If the port is not 6470, you must change it with the "lan -p 6470" command (unless you have deliberately set the port number to a different value because of a conflict).

If it takes a long time to connect to the network

☐ **Check the subnet masks on the other LAN devices connected to your network. All of the devices should be configured to use the same subnet mask.**

Subnet mask error messages do not indicate a major problem. You can continue using the HP E3472A/73A Emulator.

The HP E3472A/73A Emulator automatically sets its subnet mask based on the first subnet mask it detects on the network. If it then detects other subnet masks, it will generate error messages.

If there are many subnet masks in use on the local subnet, the HP E3472A/73A Emulator may take a very long time to connect to the network after it is turned on.

Problems with the Serial Interface

If you cannot verify RS-232 communication

If the HP E3472A/73A Emulator prompt does not appear in the terminal emulator window:

- ☐ Make sure that you have connected the HP E3472A/73A Emulator to the proper power source and that the power light is lit.

- ☐ Make sure that you have properly configured the data communications switches on the HP E3472A/73A Emulator and the data communications parameters on the host computer. You should also verify that you are using the correct cable.

  The most common type of data communications configuration problem involves the configuration of the HP E3472A/73A Emulator as a DTE device instead of as a DCE device. If you are using the wrong type of cable, no prompt will be displayed.

Caution

Use the recommended cable. If the cable is not shielded, or if the cable is not grounded at the serial controller, the HP E3472A/73A Emulator may be damaged by electrostatic discharge (Recommended cable part number is HP C2932A).

Problems with the HP E3472A/73A Emulator Itself

To execute the built-in performance verification test

In addition to the powerup tests, there are additional tests available through the built-in "terminal interface." Three of these tests can be invoked through either a **telnet** session to the HP E3472A/73A Emulator or through a terminal emulator on the RS-232 port. The LAN tests can only be executed through the RS-232 port. The HP E3472A/73A Emulator provides the tests for each of the emulation controller and emulation probe, enabling you to easily isolate a faulty device.

The remainder of this section assumes that the tests are being run from a terminal emulator connected to the RS-232 port. When using a terminal emulator via LAN, configure the emulator using the DIP switches.

Test procedure for the emulation controller

Procedure

1. Dismount the power supply from the emulation controller.
2. Remove the emulation probe.

   Disconnect the 50-pin ribbon cable and AUX power cable.
3. Set all of the DIP switches to CLOSED.

   This is standard RS-232 at 9600 baud which can be connected directly to a 9 pin RS-232 interface that conforms to the IBM PC-AT 9 pin standard.
4. Loop-back the BREAK IN and TRIGGER OUT BNC connectors by connecting a coaxial cable between them.
5. Connect the E3496-66502 loop-back board to the 50-pin connector.
6. To execute the LAN feedback tests, disconnect the LAN BNC connector from the network and terminate with two 50 ohm terminators on a tee.

7 Connect the power supply to the emulation controller.

8 Enter the **pv** command through the terminal emulator.

Options available for the "pv" are explained in the help screen displayed by typing "help pv" or "? pv" at the prompt. The help screen output will appear similar to the screen shown below:

```
c>? pv

  pv <options> <count> - Execute the performance verification diagnostics.

    pv              - display pv warning message
    pv -l           - list available pv tests only (do not execute)
    pv -d           - execute emulator subsystem tests only
    pv -t <x[-y]>   - select system test number <x> or range <x-y> only
    pv -t *         - select all system tests
    pv -d -t <x>    - select emulation subsystem test <x> only
    pv -v <verbose> - set verbose level;  valid levels: 0-9
    pv -f           - force tests to execute (HP internal use only)
    pv -n           - do not initialize system (HP internal use only)
    pv <count>      - execute diagnostics <count> number of times,
                      <count> of 0 repeats until keyboard break
  --- SYSTEM SETUP ---
    o Connect a coaxial cable between the BREAK IN and TRIGGER OUT BNCs.
    o Replace the target cable with the SELFTEST LOOPBACK connector.
    o To execute the LAN Feedback tests, disconnect the LAN BNC connector
      from the network and terminate with two 50 ohm terminators on a tee.
      (Run pv from the RS232 Port with LAN disabled)

  *** WARNING *** This command performs a system initialization after
                  all pv execution is completed.

c>
```

Examples

To execute all tests one time:

```
pv 1
```

To execute test 2 with maximum debug output repeatedly until a ^C is entered:

```
pv -t2 -v9 0
```

To execute tests 3, 4, and 5 only for 2 cycles:

```
pv -t3-5 2
```

The tests available through this command can be displayed as follows:

```
c>pv -l
  Testing: HPE3499A Series Emulation System
    Test  1: Powerup PV Results
    Test  2: LAN 10Base2 Feedback Test
    Test  3: LAN 10BaseT Feedback Test
    Test  4: Break In and Trigger Out BNC Feedback Test
    Test  5: Target Probe Feedback Test
    Test  6: Boundary Scan Master Test
    Test  7: I2C Test
c>
```

On a good system, when the E3496-66502 loop-back board is plugged into the 50-pin target connector, the RST LED will light and the BKG and USER LEDs will be out.

The results on a good system are as follows:

```
c>pv 1
  Testing: HPE3499A Series Emulation System
    Test  1: Powerup PV Results                              Passed!
    Test  2: LAN 10Base2 Feedback Test                       Passed!
    Test  3: LAN 10BaseT Feedback Test                       Passed!
    Test  4: Break In and Trigger Out BNC Feedback Test      Passed!
    Test  5: Target Probe Feedback Test                      Passed!
    Test  6: Boundary Scan Master Test                       Passed!
    Test  7: I2C Test                                        Passed!
  FAILED  Number of tests: 1          Number of failures: 0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written permission is prohibited, except as allowed under copyright laws.


  HPE3499B Series Emulation System
    Version:   A.01.00 17Aug96
    Location:  Generics

c>
```

If a failure is found on one of these tests, details of Failure can be obtained through using a verbose level of 2 or more.

TEST 2: LAN 10BASE2 Feedback Test

For LAN 10BASE2 test, the following is an example of a failure which is *not* caused by a broken HP E3472A/73A Emulator.

```
R>pv -t2 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 2: LAN 10Base2 Feedback Test                    failed!
      FAILED - no lan connection (LAN probably not terminated)
  FAILED  Number of tests: 1          Number of failures: 1
```

Check to see that the port under test has a good cable connected to it and that the cable is properly terminated with a 50 ohm terminator on each end of the overall cable.

```
R>pv -t2 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 2: LAN 10Base2 Feedback Test                    failed!
      FAILED due to excessive collisions
  FAILED  Number of tests: 1          Number of failures: 1
```

The most common cause of this problem is poor termination of the cable or failure to remove the port under test from the LAN before performing the test. Check to see that the terminators are good (50 Ohms) and that you are isolated from any traffic on a system LAN.

```
R>pv -t2 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 2: LAN 10Base2 Feedback Test                    failed!
      FAILED - invalid Ethernet address in EEPROM
  FAILED  Number of tests: 1          Number of failures: 1
```

First check to see that a correct LLA and IP address have been set in the virtual EEPROM through the "lan" command. If the "lan" command shows bad information for the LLA and IP, then try to set them to correct values.

If you are unable to set them to correct values, their is a failure in the FLASH ROM which requires service from HP.

Test 3: 10BaseT Feedback Test

```
R>pv -t3 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 3: LAN 10BaseT Feedback Test                    passed!
  PASSED  Number of tests: 1          Number of failures: 0
```

In addition to the internal checks performed in Test 2, this test also checks for shorts on the cable connected to the network. If this test fails, disconnect the cable and run the test again. If it then passes, the cable is faulty. If it still fails, it requires service from HP.

If the HP E3472A/73A Emulator passes this "pv" test, additional testing can be performed through exercising the connection to the network. To run this test, set configuration switch 1 and switch 5 to OPEN, all other configuration switches CLOSED (this enables LAN using 10BaseT). Cycle power and wait for 15 to 30 seconds. Then "ping" the HP E3472A/73A Emulator from your host computer or PC. See the LAN documentation for your host computer for the location and action of the "ping" utility. If the HP E3472A/73A Emulator fails to respond to the "ping" request, verify that the lan parameters (IP address and gateway address) are set correctly and that your host computer recognizes the IP address of the HP E3472A/73A Emulator. If all else is good, then failure to respond to ping indicates a faulty HP E3472A/73A Emulator.

TEST 4: Break In and Trigger Out BNC Feedback Test

```
R>pv -t4 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 4: Break In and Trigger Out BNC Feedback Test    failed!
      Break In not receiving Break Out HIGH
  FAILED  Number of tests: 1           Number of failures: 1
```

Before returning to HP, check to ensure that you have connected a good Coaxial cable between the two BNCs. If the cable is good, the HP E3472A/73A Emulator is bad.

TEST 5: Target Probe Feedback Test

A verbose output on this test can be extensive. For example, the following is the output of this test if you forget to plug in the E3496-66502 loop-back board.

```
p>pv -t5 -v2 1

  Testing: HPE3499A Series Emulation System
    Test # 5: Target Probe Feedback Test                    failed!
      Bad 20 Pin Status Read when unconnected = 0x7fb7
                              Expected Value = 0xffb7
      Bad 20 Pin Status Read when connected= 7fb7
                             Expected Value = 0x7fb7
```

```
     Output 19 Low not received on Input 11
     Output 11 Low not received on Input 19
     Output 13 Low not received on Input 1
     Output 12 High not received on Input 6
     Output 12 and Input 6 not pulled high on release
     Output 8 Low not received on Input 10
     Output 7 Low not received on Input 20
     Output 4 Low not received on Input 14
     Output 2 Low not received on Input 18
  FAILED  Number of tests: 1          Number of failures: 1
```

If the you get a verbose output like this, check to make sure that the self test loop-back board was connected properly.

Note

You can check the 50-pin ribbon cable by connecting it between the emulation controller and loop-back board and performing this test.

Test procedure for the emulation probe

Procedure

1. Dismount the power supply from the emulation controller.
2. Connect the emulation probe and the emulation controller.

   Connect the 50-pin ribbon cable and AUX power cable.
3. Plug the demo board into the 177-pin PGA connector.
4. Set the DIP switch on the demo board to "TEST MODE."
5. Set all of the DIP switches to CLOSED.

   This is standard RS-232 at 9600 baud which can be connected directly to a 9 pin RS-232 interface that conforms to the IBM PC-AT 9 pin standard.
6. Connect a coaxial cable between the BREAK IN and TRIGGER OUT BNCs.

   Connect the power supply to the emulation controller.
8. Enter the **pv** command through the terminal emulator.

   After testing, return the DIP switch on the demo board to the"DEMO MODE."

   The results on a good system are as follows:

```
c>pv 1
  Testing: HPE3499A Series Emulation System
    Test  1: Powerup PV Results                              Passed!
    Test  2: LAN 10Base2 Feedback Test                       Passed!
    Test  3: LAN 10BaseT Feedback Test                       Passed!
    Test  4: Break In and Trigger Out BNC Feedback Test      Passed!
    Test  5: Target Probe Feedback Test                      Passed!
```

```
    Test  6: Boundary Scan Master Test                    Passed!
    Test  7: I2C Test                                     Passed!
  Testing: HPE3472A Hitachi SH7040 Series Emulator
    Test  1: Monitor Memory Test                          Passed!
    Test  2: Mapper Memory Test                           Passed!
    Test  3: Run Control Test                             Passed!
    Test  4: On-Chip ROM Test                             Passed!
    Test  5: On-Chip RAM Test                             Passed!
    Test  6: Emulation Memory Test                        Passed!
    Test  7: Target Interface Feedback Test               Passed!
    Test  8: Analyzer Interface Test                      Passed!
  FAILED  Number of tests: 1          Number of failures: 0


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written permission is prohibited, except as allowed under copyright laws.


  HPE3499B Series Emulation System
    Version:   A.01.00 17Aug96
    Location:  Generics

  HPE3472A Hitachi SH7040 Series Emulator
    Version:   A.01.00 17Aug96
    Speed:     33.3 MHz
    Memory:    0 KBytes
    PC Board:  f200-00e0-0000-78ff

c>
```

If a failure is found on one of these tests, details of Failure can be obtained through using a verbose level of 2 or more.

If the data in ROM is corrupt

Sometimes the data in the FLASH ROM can be corrupt. This can be caused while programming of the FLASH ROM if one of the following things happens:

- A system fault
- A loss of power to the HP E3472A/73A Emulator or host computer
- A break in the communications channel

If this happens, try the following steps:

1. **Cycle power on the HP E3472A/73A Emulator and try the flash programming utility (progflash) again.**

   If this doesn't work, continue with the next step:

2. **Set switch S4 to OPEN, then cycle power.**

   This will force the HP E3472A/73A Emulator to use only the boot ROM. Try running the programming utility again. If this is successful, return the switches to their normal configuration (S3 and S4 CLOSED) and cycle power.

Note

A

Registers List

HP E3472A

The HP E3472A Emulator has the following register classes.

*	Basic registers
intc	Interrupt controller
ubc	User break controller
dtc	Data transfer controller
cac	Cache controller
bsc	Bus state controller
dmac0	DMA controller 0
dmac1	DMA controller 1
dmac2	DMA controller 2
dmac3	DMA controller 3
mtu0	Multi-function timer pulse unit 0
mtu1	Multi-function timer pulse unit 1
mtu2	Multi-function timer pulse unit 2
mtu3	Multi-function timer pulse unit 3
mtu4	Multi-function timer pulse unit 4
wdt	Watch-dog timer
sci0	Serial communication interface 0
sci1	Serial communication interface 1
adc	A/D converter
cmt0	Compare match timer 0
cmt1	Compare match timer 1
pfc	Pin function controller
port	I/O port
poe	Port output enable
sys	System control

The following list shows registers included in each register class.

- Basic registers (*)

pc	Program counter
sr	Status register
r0	General purpose register 0
r1	General purpose register 1
r2	General purpose register 2
r3	General purpose register 3
r4	General purpose register 4
r5	General purpose register 5
r6	General purpose register 6
r7	General purpose register 7
r8	General purpose register 8
r9	General purpose register 9
r10	General purpose register 10
r11	General purpose register 11
r12	General purpose register 12
r13	General purpose register 13
r14	General purpose register 14
r15	General purpose register 15
sp	Hardware stack pointer
gbr	Global base register
vbr	Vector base register
pr	Procedure register
mach	Multiple and accumulate register H
macl	Multiple and accumulate register L

- Interrupt controller (intc)

ipra	Interrupt priority register A
iprb	Interrupt priority register B
iprc	Interrupt priority register C
iprd	Interrupt priority register D
ipre	Interrupt priority register E
iprf	Interrupt priority register F
iprg	Interrupt priority register G
iprh	Interrupt priority register H
icr	Interrupt control register
isr	IRQ status register

- User break controller (ubc)

ubar	User break address register
ubamr	User break address mask register
ubbr	User break bus cycle register

- Data transfer controller (dtc)

dtea	DTC enable register A
dteb	DTC enable register B
dtec	DTC enable register C
dted	DTC enable register D
dtee	DTC enable register E
dtcsr	DTC control/status register
dtbr	DTC data base register

- Cache controller (cac)

ccr	Cache control register

- Bus state controller (bsc)

bcr1	Bus control register 1
bcr2	Bus control register 2
wcr1	Wait control register 1
wcr2	Wait control register 2
dcr	DRAM area control register
rtcsr	Refresh timer control/status register
rtcnt	Refresh timer counter
rtcor	Refresh timer constant register

- DMA controller 0 (dmac0)

dmaor	DMA operation register
sar0	DMA source address register 0
dar0	DMA destination address register 0
dmatcr0	DMA transfer count register 0
chcr0	DMA channel control register 0

- DMA controller 1 (dmac1)

dmaor	DMA operation register
sar1	DMA source address register 1
dar1	DMA destination address register 1
dmatcr1	DMA transfer count register 1
chcr1	DMA channel control register 1

- DMA controller 2 (dmac2)

dmaor	DMA operation register
sar2	DMA source address register 2
dar2	DMA destination address register 2
dmatcr2	DMA transfer count register 2
chcr2	DMA channel control register 2

- DMA controller 3 (dmac3)

dmaor	DMA operation register
sar3	DMA source address register 3
dar3	DMA destination address register 3
dmatcr3	DMA transfer count register 3
chcr3	DMA channel control register 3

- Multi-function timer pulse unit 0 (mtu0)

tstr	Timer start register
tsyr	Timer synchronization register
tcr0	Timer control register 0
tmdr0	Timer mode register 0
tior0	Timer I/O control register 0
tier0	Timer interrupt enable register 0
tsr0	Timer status register 0
tcnt0	Timer counter 0
tgr0a	General register 0A
tgr0b	General register 0B
tgr0c	General register 0C
tgr0d	General register 0D

- Multi-function timer pulse unit 1 (mtu1)

tstr	Timer start register
tsyr	Timer synchronization register
tcr1	Timer control register 1
tmdr1	Timer mode register 1
tior1	Timer I/O control register 1
tier1	Timer interrupt enable register 1
tsr1	Timer status register 1
tcnt1	Timer counter 1
tgr1a	General register 1A
tgr1b	General register 1B

- Multi-function timer pulse unit 2 (mtu2)

tstr	Timer start register
tsyr	Timer synchronization register
tcr2	Timer control register 2
tmdr2	Timer mode register 2
tior2	Timer I/O control register 2
tier2	Timer interrupt enable register 2
tsr2	Timer status register 2
tcnt2	Timer counter 2
tgr2a	General register 2A
tgr2b	General register 2B

- Multi-function timer pulse unit 3 (mtu3)

tstr	Timer start register
tsyr	Timer synchronization register
toer	Timer output master enable register
tocr	Timer output control register
tgcr	Timer gate control register
tcdr	Timer cycle data register
tddr	Timer dead time data register
tcnts	Timer sub-counter (for reference only)
tcbr	Timer cycle buffer register
tcr3	Timer control register 3
tmdr3	Timer mode register 3
tior3	Timer I/O control register 3
tier3	Timer interrupt enable register 3
tsr3	Timer status register 3
tcnt3	Timer counter 3
tgr3a	General register 3A
tgr3b	General register 3B
tgr3c	General register 3C
tgr3d	General register 3D

- Multi-function timer pulse unit 4 (mtu4)

tstr	Timer start register
tsyr	Timer synchronization register
toer	Timer output master enable register
tocr	Timer output control register
tgcr	Timer gate control register
tcdr	Timer cycle data register
tddr	Timer dead time data register
tcnts	Timer sub-counter
tcbr	Timer cycle buffer register
tcr4	Timer control register 4
tmdr4	Timer mode register 4
tior4	Timer I/O control register 4
tier4	Timer interrupt enable register 4
tsr4	Timer status register 4
tcnt4	Timer counter4
tgr4a	General register 4A
tgr4b	General register 4B
tgr4c	General register 4C
tgr4d	General register 4D

- Watch-dog timer (wdt)

wdtcsr	Timer control/status register
wdtcnt	Timer counter
rstcsr	Reset control/status register

- Serial communication interface 0 (sci0)

smr0	Serial mode register 0
brr0	Bit rate register 0
scr0	Serial control register 0
tdr0	Transmit data register 0
ssr0	Serial status register 0
rdr0	Receive data register 0 (for reference only)

- Serial communication interface 1 (sci1)

smr1	Serial mode register 1
brr1	Bit rate register 1
scr1	Serial control register 1
tdr1	Transmit data register 1
ssr1	Serial status register 1
rdr1	Receive data register 1 (for reference only)

- A/D converter (adc)

addra	A/D data register A (for reference only)
addrb	A/D data register B (for reference only)
addrc	A/D data register C (for reference only)
addrd	A/D data register D (for reference only)
addre	A/D data register E (for reference only)
addrf	A/D data register F (for reference only)
addrg	A/D data register G (for reference only)
addrh	A/D data register H (for reference only)
adcsr	A/D control/status register
adcr	A/D control register

- Compare match timer0 (cmt0)

cmstr	Compare match timer start register
cmcsr0	Compare match timer control/status register 0
cmcnt0	Compare match timer counter 0
cmcor0	Compare match timer constant register 0

- Compare match timer1 (cmt1)

cmstr	Compare match timer start register
cmcsr1	Compare match timer control/status register 1
cmcnt1	Compare match timer counter 1
cmcor1	Compare match timer constant register 1

- Pin function controller (pfc)

paior	Port A IO register
pacrh	Port A control register H
pacrl1	Port A control register L1
pacrl2	Port A control register L2
pbior	Port B IO register
pbcr1	Port B control register 1
pbcr2	Port B control register 2
pcior	Port C IO register
pccr	Port C control register
pdior	Port D IO register
pdcrh1	Port D control register H1
pdcrh2	Port D control register H2
pdcr1	Port D control register L
peior	Port E IO register
pecr1	Port E control register 1
pecr2	Port E control register 2
ifcr	IRQOUT function control register

- I/O port (port)

padr	Port A data register
pbdr	Port B data register
pcdr	Port C data register
pddr	Port D data register
pedr	Port E data register
pfdr	Port F data register (for reference only)

- Port output enable (poe)

icsr	Input level control/status register
ocsr	Output level control/status register

- System control (sys)

sbycr	Standby control register

HP E3473A

The HP E3473A Emulator has the following register classes.

*	Basic registers
intc	Interrupt controller
ubc	User break controller
bsc	Bus state controller
dmac0	DMA controller 0
dmac1	DMA controller 1
dmac2	DMA controller 2
dmac3	DMA controller 3
atu0	Advanced timer unit 0
atu1	Advanced timer unit 1
atu2	Advanced timer unit 2
atu3	Advanced timer unit 3
atu4	Advanced timer unit 4
atu5	Advanced timer unit 5
atu6	Advanced timer unit 6
atu7	Advanced timer unit 7
atu8	Advanced timer unit 8
atu9	Advanced timer unit 9
atu10	Advanced timer unit 10
apc	Advanced pulse controller
wdt	Watch-dog timer
cmt0	Compare match timer 0
cmt1	Compare match timer 1
sci0	Serial communication interface 0
sci1	Serial communication interface 1
sci2	Serial communication interface 2
adc	A/D converter
pfc	Pin function controller
port	I/O port
sys	System control

The following list shows registers included in each register class.

- Basic registers (*)

pc	Program counter
sr	Status register
r0	General purpose register 0
r1	General purpose register 1
r2	General purpose register 2
r3	General purpose register 3
r4	General purpose register 4
r5	General purpose register 5
r6	General purpose register 6
r7	General purpose register 7
r8	General purpose register 8
r9	General purpose register 9
r10	General purpose register 10
r11	General purpose register 11
r12	General purpose register 12
r13	General purpose register 13
r14	General purpose register 14
r15	General purpose register 15
sp	Hardware stack pointer
gbr	Global base register
vbr	Vector base register
pr	Procedure register
mach	Multiple and accumulate register H
macl	Multiple and accumulate register L

- Interrupt controller (intc)

ipra	Interrupt priority register A
iprb	Interrupt priority register B
iprc	Interrupt priority register C
iprd	Interrupt priority register D
ipre	Interrupt priority register E
iprf	Interrupt priority register F
iprg	Interrupt priority register G
iprh	Interrupt priority register H
icr	Interrupt control register
isr	IRQ status register

- User break controller (ubc)

ubar	User break address register
ubamr	User break address mask register
ubbr	User break bus cycle register

- Bus state controller (bsc)

bcr1	Bus control register 1
bcr2	Bus control register 2
wcr1	Wait control register 1
wcr2	Wait control register 2

- DMA controller 0 (dmac0)

dmaor	DMA operation register
sar0	DMA source address register 0
dar0	DMA destination address register 0
dmatcr0	DMA transfer count register 0
chcr0	DMA channel control register 0

- DMA controller 1 (dmac1)

dmaor	DMA operation register
sar1	DMA source address register 1
dar1	DMA destination address register 1
dmatcr1	DMA transfer count register 1
chcr1	DMA channel control register 1

- DMA controller 2 (dmac2)

dmaor	DMA operation register
sar2	DMA source address register 2
dar2	DMA destination address register 2
dmatcr2	DMA transfer count register 2
chcr2	DMA channel control register 2

- DMA controller 3 (dmac3)

dmaor	DMA operation register
sar3	DMA source address register 3
dar3	DMA destination address register 3
dmatcr3	DMA transfer count register 3
chcr3	DMA channel control register 3

- Advanced timer unit 0 (atu0)

tstr	Timer start register
pscr1	Pre-scaler register 1
tior0a	Timer I/O control register 0A
tgsr	Trigger selection register
itvrr	Interval interrupt request register
tsrah	Timer status register AH
tsral	Timer status register AL
tiera	Timer interrupt enable register A
tcnt0	Free learning counter 0
icr0a	Input capture register 0A
icr0b	Input capture register 0B
icr0c	Input capture register 0C
icr0d	Input capture register 0D

- Advanced timer unit 1 (atu1)

tstr	Timer start register
pscr1	Pre-scaler register 1
tcr1	Timer control register 1
tior1a	Timer I/O control register 1A
tior1b	Timer I/O control register 1B
tior1c	Timer I/O control register 1C
tsrb	Timer status register B
tierb	Timer interrupt enable register B
tcnt1	Free learning counter 1
gr1a	General register 1A
gr1b	General register 1B
gr1c	General register 1C
gr1d	General register 1D
gr1e	General register 1E
gr1f	General register 1F
osbr	Offset base register

- Advanced timer unit 2 (atu2)

tstr	Timer start register
pscr1	Pre-scaler register 1
tcr2	Timer control register 2
tior2a	Timer I/O control register 2A
tsrc	Timer status register C
tierc	Timer interrupt enable register C
tcnt2	Free learning counter 2
gr2a	General register 2A
gr2b	General register 2B

- Advanced timer unit 3 (atu3)

tstr	Timer start register
pscr1	Pre-scaler register 1
tmdr	Timer mode register
tsrdh	Timer status register DH
tsrdl	Timer status register DL
tierdh	Timer interrupt enable register DH
tierdl	Timer interrupt enable register DL
tcr3	Timer control register 3
tior3a	Timer I/O control register 3A
tior3b	Timer I/O control register 3B
tcnt3	Free learning counter 3
gr3a	General register 3A
gr3b	General register 3B
gr3c	General register 3C
gr3d	General register 3D

- Advanced timer unit 4 (atu4)

tstr	Timer start register
pscr1	Pre-scaler register 1
tmdr	Timer mode register
tsrdh	Timer status register DH
tsrdl	Timer status register DL
tierdh	Timer interrupt enable register DH
tierdl	Timer interrupt enable register DL
tcr4	Timer control register 4
tior4a	Timer I/O control register 4A
tior4b	Timer I/O control register 4B
tcnt4	Free learning counter 4
gr4a	General register 4A
gr4b	General register 4B
gr4c	General register 4C
gr4d	General register 4D

- Advanced timer unit 5 (atu5)

tstr	Timer start register
pscr1	Pre-scaler register 1
tmdr	Timer mode register
tsrdh	Timer status register DH
tsrdl	Timer status register DL
tierdh	Timer interrupt enable register DH
tierdl	Timer interrupt enable register DL
tcr5	Timer control register 5
tior5a	Timer I/O control register 5A
tcnt5	Free learning counter 5
gr5a	General register 5A
gr5b	General register 5B

- Advanced timer unit 6 (atu6)

tstr	Timer start register
pscr1	Pre-scaler register 1
tsre	Timer status register E
tiereh	Timer interrupt enable register EH
tierel	Timer interrupt enable register EL
tcr6	Timer control register 6
tcnt6	Free learning counter 6
cylr6	Cycle register 6
bfr6	Buffer register 6
dtr6	Duty register 6

- Advanced timer unit 7 (atu7)

tstr	Timer start register
pscr1	Pre-scaler register 1
tsre	Timer status register E
tiereh	Timer interrupt enable register EH
tierel	Timer interrupt enable register EL
tcr7	Timer control register 7
tcnt7	Free learning counter 7
cylr7	Cycle register 7
bfr7	Buffer register 7
dtr7	Duty register 7

- Advanced timer unit 8 (atu8)

tstr	Timer start register
pscr1	Pre-scaler register 1
tsre	Timer status register E
tiereh	Timer interrupt enable register EH
tierel	Timer interrupt enable register EL
tcr8	Timer control register 8
tcnt8	Free learning counter 8
cylr8	Cycle register 8
bfr8	Buffer register 8
dtr8	Duty register 8

- Advanced timer unit 9 (atu9)

tstr	Timer start register
pscr1	Pre-scaler register 1
tsre	Timer status register E
tiereh	Timer interrupt enable register EH
tierel	Timer interrupt enable register EL
tcr9	Timer control register 9
tcnt9	Free learning counter 9
cylr9	Cycle register 9
bfr9	Buffer register 9
dtr9	Duty register 9

- Advanced timer unit 10 (atu10)

pscr1	Pre-scaler register 1
tcr10	Timer control register 10
tsrf	Timer status register F
tierf	Timer interrupt enable register F
dstr	Down count start register
tcnr	Timer connection register
dcnt10a	Down counter 10A
dcnt10b	Down counter 10B
dcnt10c	Down counter 10C
dcnt10d	Down counter 10D
dcnt10e	Down counter 10E
dcnt10f	Down counter 10F
dcnt10g	Down counter 10G
dcnt10h	Down counter 10H

- Advanced pulse controller (apc)

popcr	Pulse output port control register

- Watch-dog timer (wdt)

wdtcsr	Timer control/status register
wdtcnt	Timer counter
rstcsr	Reset control/status register

- Compare match timer0 (cmt0)

cmstr	Compare match timer start register
cmcsr0	Compare match timer control/status register 0
cmcnt0	Compare match timer counter 0
cmcor0	Compare match timer constant register 0

- Compare match timer1 (cmt1)

cmstr	Compare match timer start register
cmcsr1	Compare match timer control/status register 1
cmcnt1	Compare match timer counter 1
cmcor1	Compare match timer constant register 1

- Serial communication interface 0 (sci0)

smr0	Serial mode register 0
brr0	Bit rate register 0
scr0	Serial control register 0
tdr0	Transmit data register 0
ssr0	Serial status register 0
rdr0	Receive data register 0 (for reference only)

- Serial communication interface 1 (sci1)

smr1	Serial mode register 1
brr1	Bit rate register 1
scr1	Serial control register 1
tdr1	Transmit data register 1
ssr1	Serial status register 1
rdr1	Receive data register 1 (for reference only)

- Serial communication interface 2 (sci2)

smr2	Serial mode register 2
brr2	Bit rate register 2
scr2	Serial control register 2
tdr2	Transmit data register 2
ssr2	Serial status register 2
rdr2	Receive data register 2 (for reference only)

- A/D converter (adc)

addr0	A/D data register 0 (for reference only)
addr1	A/D data register 1 (for reference only)
addr2	A/D data register 2 (for reference only)
addr3	A/D data register 3 (for reference only)
addr4	A/D data register 4 (for reference only)
addr5	A/D data register 5 (for reference only)
addr6	A/D data register 6 (for reference only)
addr7	A/D data register 7 (for reference only)
addr8	A/D data register 8 (for reference only)
addr9	A/D data register 9 (for reference only)
addr10	A/D data register 10 (for reference only)
addr11	A/D data register 11 (for reference only)
addr12	A/D data register 12 (for reference only)
addr13	A/D data register 13 (for reference only)
addr14	A/D data register 14 (for reference only)
addr15	A/D data register 15 (for reference only)
adcsr0	A/D control/status register 0
adcr0	A/D control register 0
adcsr1	A/D control/status register 1
adcr1	A/D control register 1
adtrgr	A/D trigger register

- Pin function controller (pfc)

paior	Port A IO register
pacr	Port A control register
pbior	Port B IO register
pbcr	Port B control register
pcior	Port C IO register
pccr1	Port C control register 1
pccr2	Port C control register 2
pdior	Port D IO register
pdcr	Port D control register
peior	Port E IO register
pecr	Port E control register
pfior	Port F IO register
pfcr1	Port F control register 1
pfcr2	Port F control register 2
pgior	Port G IO register
pgcr1	Port G control register 1
pgcr2	Port G control register 2

- I/OPort (port)

padr	Port A data register
pbdr	Port B data register
pcdr	Port C data register
pddr	Port D data register
pedr	Port E data register
pfdr	Port F data register
pgdr	Port G data register
phdr	Port H data register (for reference only)

- System control (sys)

sbycr	Standby control register
syscr	System control register

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